CSS68HC68W1

May 2003

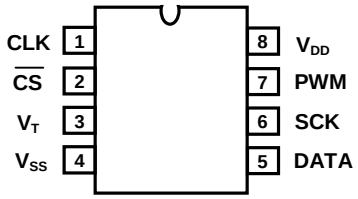
CMOS Serial Digital Pulse Width Modulator

Features

- **Direct Replacement for Intersil CDP68HC68W1**
- **Programmable Frequency and Duty Cycle Output**
- **Serial Bus Input; Compatible with Motorola/Intersil SPI Bus, Simple Shift-Register Type Interface**
- **8 Lead PDIP and SOIC Packages (Note #1)**
- **Schmitt Trigger Clock Inputs**
- **3V / 5V Operation, -40°C to 85°C Temperature Range**
- **25 MHz Clock Input Frequency**

Pinout

PDIP / SOIC (Note #1)
TOP VIEW

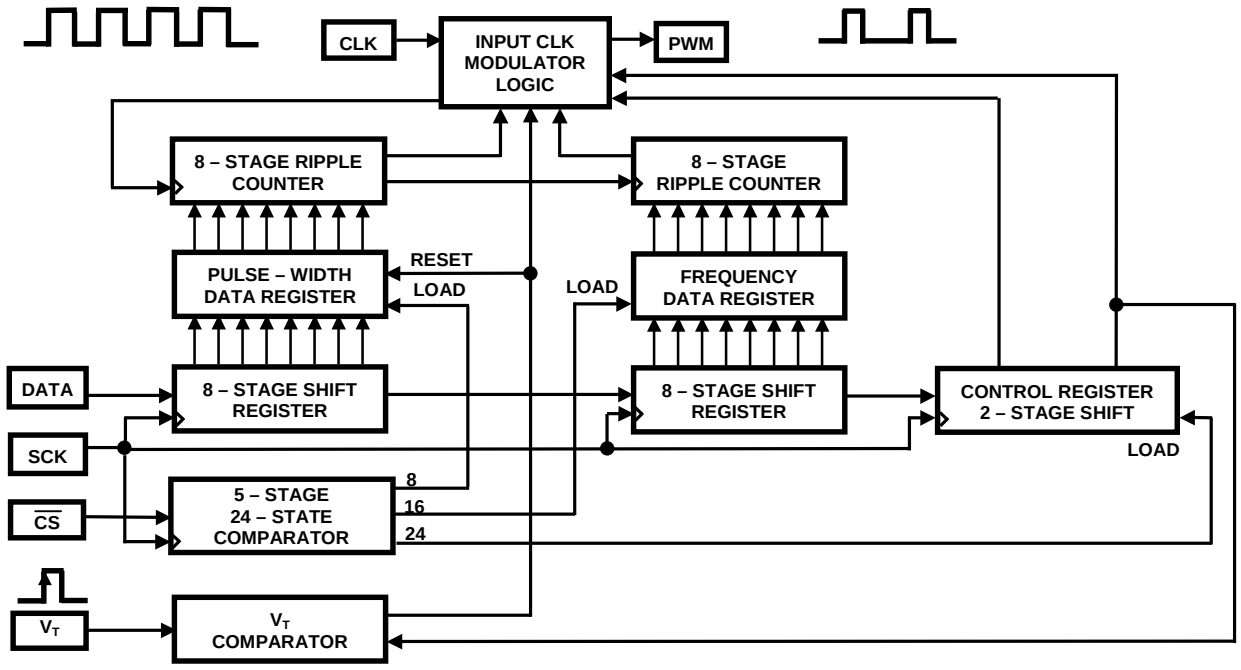


Note #1: Contact CSS for SOIC availability

Description

The CSS68HC68W1 modulates an input clock to provide a variable frequency and variable duty-cycle output signal. Three 8-bit registers (pulse width, frequency and control) are accessed via a 3 line serial interface.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; Follow proper IC Handling Procedures.

Custom Silicon Solutions, Inc. 17951 Sky Park Circle, Suite F, Irvine, CA 92614 Phone 949.797.9220 Fax 949.797.9225

Absolute Maximum Ratings

VDD Supply Voltage Range ..... -0.5V to +7V
(Referenced to V_{SS} Terminal)
Input Voltage Range..... -0.5V to V_{DD} +0.5V
Input Injection Current, Any One Input.....±25mA

Operating Conditions

Temperature Range (T_A) ..... -40°C to 85°C

T_A = Full Package Temperature Range

Thermal Information

Thermal Resistance θ_{JA} (Typical, Note 2) .....99 (°C/W)
Maximum Output Power Dissipation 100mW
Maximum Storage Temperature Range (T_{STG}).....-65°C to 150°C
Maximum Lead Temperature (During Soldering).....265°C
At Distance 1/16 ± 1/32 IN. (1.59 ± 0.79mm)
From Case for 10s Max

CAUTION: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE:
2) θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3) Typical values are for operation at 3V or 5V, 25C.

DC Electrical Specifications T_A = -40ºC to 85ºC

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 2.7V to 6.0V					
Input Voltage High Range (Except V_T)	V_{IH}	0.7*V_{DD}	0.5*V_{DD}	V_{DD}+0.3V	V
Input Voltage Low Range (Except V_T)	V_{IL}	-0.3V	0.5*V_{DD}	0.3*V_{DD}	V
Input Leakage Current	I_{IN}	-	-	±1	µA
Clock Input Capacitance	C_{IN}	-	-	10	pF
Supply Current (Power Down Mode, Clock Disabled)	I_{PD}		< 0.01	1	µA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 2.7V to 3.3V					
Input Hysteresis (CLK & SCK)	V_{HYST}	-	0.65	-	V
V_T Pin Input Voltage Threshold	V_{IT}	0.1*V_{DD}	0.128*V_{DD}	0.15*V_{DD}	V
Low Level Output Voltage (I_{OL} = 1.0mA)	V_{OL}	-	0.1	0.4	V
High Level Output Voltage (I_{OH} = 1.0mA)	V_{OH}	V_{DD} – 0.4V	V_{DD} – 0.15V	-	V
Operating Device Current (f_{CLK} = 1MHz)	I_{OPER}	-	0.05	0.1	mA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 4.0V to 6.0V					
Input Hysteresis (CLK & SCK)	V_{HYST}	-	0.9	-	V
V_T Pin Input Voltage Threshold	V_{IT}	0.1*V_{DD}	0.125*V_{DD}	0.15*V_{DD}	V
Low Level Output Voltage (I_{OL} = 1.6mA)	V_{OL}	-	0.1	0.4	V
High Level Output Voltage (I_{OH} = 1.6mA)	V_{OH}	V_{DD} – 0.4V	V_{DD} – 0.15V	-	V
Operating Device Current (f_{CLK} = 1MHz)	I_{OPER}	-	0.15	0.35	mA

Control Timing T_A = -40°C to 85°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 2.7V to 3.3V					
Clock Frequency	F_{CLK}	DC	30	15	MHz
Cycle Time	t_{CYC}	-	-	-	ns
Clock to PWM Out	t_{PWMO}	-	20	125	ns
Clock High Time	t_{CLKH}	50	15	-	ns
Clock Low Time	t_{CLKL}	50	15	-	ns
Clock Rise Time (20% V_{DD} to 70% V_{DD})	t_R	-	-	100	ns
Clock Fall Time (70% V_{DD} to 20% V_{DD})	t_F	-	-	100	ns

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 4.0V to 6.0V					
Clock Frequency	F_{CLK}	DC	40	25	MHz
Cycle Time	t_{CYC}	-	-	-	ns
Clock to PWM Out	t_{PWMO}	-	15	125	ns
Clock High Time	t_{CLKH}	50	10	-	ns
Clock Low Time	t_{CLKL}	50	10	-	ns
Clock Rise Time (20% V_{DD} to 70% V_{DD})	t_R	-	-	100	ns
Clock Fall Time (70% V_{DD} to 20% V_{DD})	t_F	-	-	100	ns

SPI Interface Timing T_A = -40°C to 85°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DD} = 2.7V to 6.0V					
Serial Clock Frequency	f_{SCK}	DC	40	10	MHz
Cycle Time	t_{SCYC}	100	25	-	ns
Enable Lead Time	t_{ELD}	25	5	-	ns
Enable Lag Time	t_{ELG}	-	10	50	ns
Serial Clock (SCK) High Time	t_{SH}	50	10	-	ns
Serial Clock (SCK) Low Time	t_{SL}	50	10	-	ns
Data Setup Time	t_{DSU}	30	15	-	ns
Data Hold Time	t_{DHD}	15	5	-	ns
Fall Time (70% V_{DD} to 20% V_{DD})	t_{SCKF}	-	-	100	ns
Rise Time (70% V_{DD} to 20% V_{DD})	t_{SCKR}			100	ns

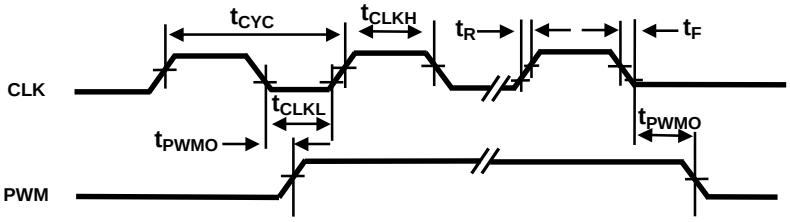


FIGURE 1. PWM TIMING

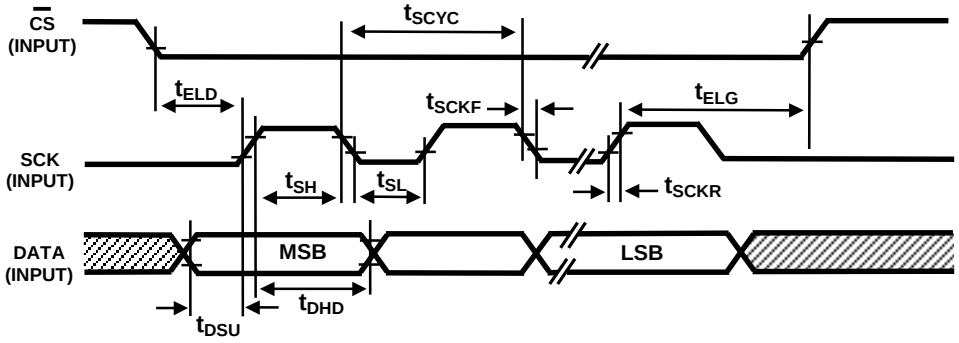


FIGURE 2. SERIAL PERIPHERAL INTERFACE TIMING

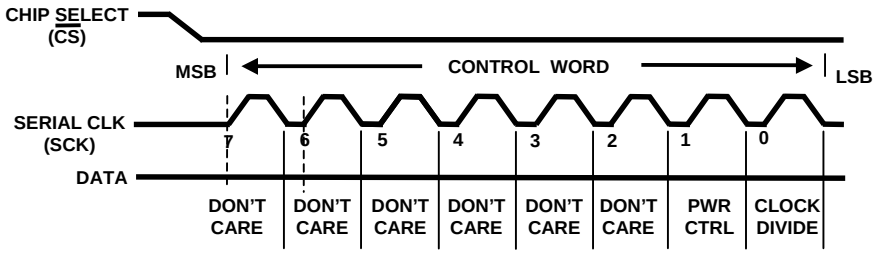


FIGURE 3A. CONTROL WORD

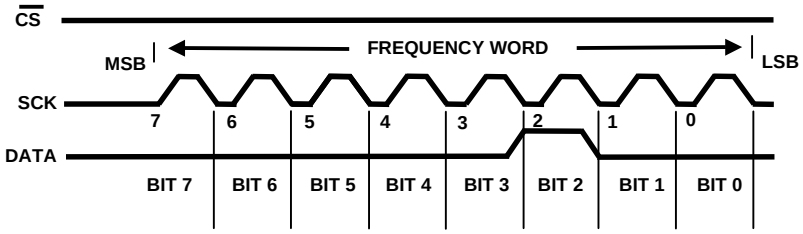


FIGURE 3B. FREQUENCY WORD

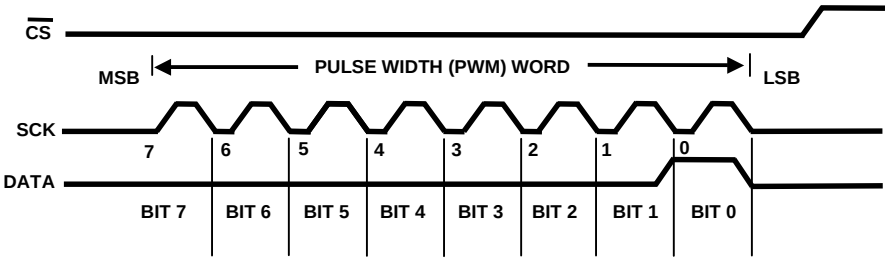


FIGURE 3C. PULSE WIDTH WORD

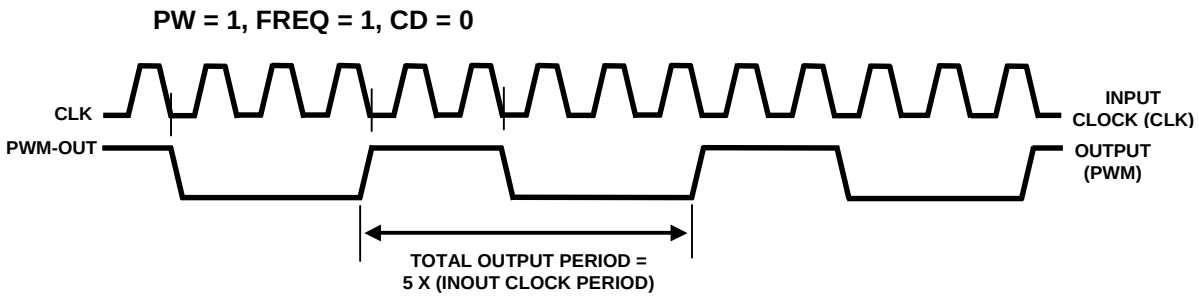


FIGURE 3D. CSS68HC68W1 INTERFACE TIMING SPECIFICATIONS

Introduction

The digital pulse width modulator (DPWM) divides down a clock signal supplied via the CLK input as specified by the control, frequency, and pulse width data registers. The resultant output signal, with altered frequency and duty cycle, appears at the output of the device on the PWM pin.

Functional Pin Description

V_{DD} and V_{SS}

These pins are used to supply power and establish logic levels within the PWM. V_{DD} is a positive voltage with respect to V_{SS} (ground).

CLK

The CLK pin is an input only pin where the clock signal to be altered by the PWM circuitry is supplied. This is the source of the PWM output. This input frequency can be internally divided by either one or two, depending on the state of the CD bit in the control register.

CS

The CS pin is the chip select input to the PWM's SPI interface. A high-to-low (1 to 0) transition selects the chip. A low-to-high (0 to 1) transition deselects the chip and transfers data from the shift registers to the data registers.

VT

The VT pin is the input to the voltage threshold comparator on the PWM. An analog voltage greater than $0.15*V_{DD}$ on this pin will immediately cause the PWM output to go to logic "0". This will be the status until the V_T input is returned to a voltage below $0.1*V_{DD}$, the W1 is selected, and then one or more of the data registers is written to.

An analog voltage on this pin less than 0.5V (at V_{DD} = 5V) will allow the device to operate as specified by the values in the registers.

DATA

Data input at this pin is clocked into the shift register (i.e., latched) on the rising edge of the serial clock (SCK), most significant bits first.

SCK

The SCK pin is the serial clock input to the PWM's SPI interface. A rising edge on this pin will shift data available at the (DATA) pin into the shift register.

PWM

This pin provides the resultant output frequency and pulse width. After V_{DD} power up, the output on this pin will remain a logic "0", until the chip is selected, 24 bits of information are clocked in, and the chip is deselected.

Functional Description

Serial Port

Data is entered into the three DPWM registers serially through the DATA pin, accompanied by a clock signal applied to the SCK. The user can supply these serial data via shift register(s) or a microcontroller's serial port, such as the SPI port available on most CSS68HD05 microcontrollers. Microcontroller I/O lines can also be used to simulate a serial port.

Data is written serially, most significant bit first, in 8, 16 or 24-bit increments. Data is sampled and shifted into the PWMs shift register on each rising edge of the SCK. The serial clock must be low when initiating a write cycle. Therefore, when using a 68HC05 microcontroller's SPI port to provide data, program the microcontroller's SPI control register bit CPOL, CPHA to 0,0.

The CSS68HC68W1 latches data words after the device is deselected. Therefore, CS must go high (inactive) following each write to the W1.

Power-Up Initialization

Upon V_{DD} power up, the output of the PWM chip will remain at a low level (logic zero) until:

1. The chip is selected (CS pin pulled low).
2. 24-bits of information are shifted in.
3. The chip is deselected (CS pin pulled high).

The 24-bits of necessary information pertain to the loading of the PWM 8-bit registers, in the following order:

1. Control register
2. Frequency register
3. Pulse width register

See section entitled ***Pulse Width Modulator Data Registers*** for a description of each register. Once initialized, the specified PWM output signal will appear until the device is reprogrammed or the voltage on the VT pin rises above the specified threshold. Reprogramming the device will update the PWM output after the end of the present output clock period.

Reprogramming Shortcuts

After the device has been fully programmed upon power up it is only necessary to input 8 bits of information to alter the output pulse width, or 16 bits to alter the output frequency.

Altering the Pulse Width: The pulse width may be changed by selecting the chip, inputting 8 bits, and deselecting the chip. By deselecting the chip, data from the first 8-bit shift register are latched into the pulse width register (PWM register). The frequency and control registers remain unchanged. The updated PWM information will appear at the output only after the end of the previous total output period.

Altering the Frequency: The frequency can be changed by selecting the chip, inputting 16 bits (frequency information followed by pulse width information), and deselecting the chip. Deselection will transfer 16 bits of data from the shift register into the frequency register and PW register. The updated frequency and PW information will appear at the PWM output pin only after the end of the previous total output period.

Altering the Control Word: Changing the clock divider and/or power control bit in the CSSHC68W1 control register requires full 24-bit programming, as described under Power Up Initialization.

Pulse Width Modulator Data Registers

Byte 1: Control Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PC	CD

B7-B2 Unused; “don’t care”.

B1, PC Power Control Bit. If this bit is a “0”, the chip will remain in the active state. If this bit is set to a “1”, internal clocking, the voltage comparator (VT) circuit and the voltage reference will be disabled. Thus the chip will enter a low current mode. The chip may only reenter the active mode by clearing this bit by clocking in a full 24 bits of information.

B0, CD Clock Driver Bit. If this bit is a “0”, the chip will set internal clocking (CLK) at a divide-by-one rate with respect to the (CLK). If this bit is set to a “1”, the internal clocking will be set to divide-by-2 state.

Byte 2: Frequency Data Register

7	6	5	4	3	2	1	0
Frequency Register							

B7-B0 This register contains the value that will determine the output frequency or total period by:

$F_{OUT} = F_{IN} / ((N+1)(CD+1))$

F_{OUT} = resultant PWM output frequency

F_{IN} = the frequency of input CLK

N = value in frequency register

CD = value of clock divider bit in control register

For a case of N (binary value in frequency register) equal to 5, CD (clock divider) = 0 (divide-by-1), the PWM output will be a frequency 1/6 that of the input clock (CLK). Likewise, the output clock period will be equal to 6 input CLK periods.

Byte 3: Pulse Width Data Register

7	6	5	4	3	2	1	0
Pulse Width Register							

B7-B0 This register contains the value that will determine the pulse width or duty cycle (high duration) of the output PWM waveform.

PW = (N+1) (CD+1)

PW = Pulse width out as measured in number of input CLK periods.

CD = Value of clock divider bit in control register.

N = Value in PW register.

For a case of N (binary value in PW register) equal to 3 and CD (clock divider) = 0 (divide-by-1), the output will be 4 input clock periods of a high level followed by the remaining clocks of the total period which will be a low level.

Assuming the frequency register contains a value of 5, the resultant PWM output would be high for 4 CLK periods, low for 2.

Using the CSS68HC68W1

Programming the CSS68HC68W1

1. Select chip
2. Write to control register
3. Write to frequency register
4. Write to pulse width register
5. Deselect chip

NEXT - TO then alter the pulse width

1. Select chip
2. Write to pulse width register*
3. Deselect chip

OR – To then alter the frequency (and possibly PW):

1. Select chip
2. Write to frequency register*
3. Write to pulse width register*
4. Deselect chip

NOTE: All writes use 8-bit words

Example

When CD = 0, frequency register = 4, pulse width register = 1; output = high for 2 input CLK periods, low for 3;

1. Select chip
2. Then write (most significant bit first) to the control, the frequency, and pulse width registers (control = 00, frequency = 04, PW = 1)
3. Deselect the chip

New pulse width out begins and PWM goes high when CS is raised after the last SCK pulse (assuming no previous time-out). PWM then toggles on falling CLK edges.

Resulting output waveform: Control = 00 = Divide-by-1, frequency = 4;

PW = 1: (1+1) (0+1) = 2 CLKs high time.

Frequency = (INPCLK) / ((04 + 1)(0+1)) = INPCLK / 5