CSS555/C CSS555C PART DESCRIPTION

The CSS555 is a micro-power version of the popular 555 Timer IC. It is pin-for-pin compatible with the standard 555 timer and features an operating current under 5µA. Its minimum supply voltage is 1.2V, making it ideal for battery-operated applications. A six-decade programmable counter is included to allow generation of long timing delays. The analog circuits are temperature compensated to provide excellent stability over a wide temperature range. Configuration data for the counter is held in EEPROM. A straightforward four-wire interface provides Read/Write access to the memory. The CSS555C device includes an internal 100pF timing capacitor. Block diagrams of the standard 555 IC and the CSS555C are shown below.
CSS555(C)  Application Circuits

Application Circuits

The following 555 timer circuits have been assembled to help show the advantages of the CSS555C timer. Its advanced features offer unique capabilities that can reduce power, decrease PCB area and eliminate the external timing capacitor. These circuits demonstrate many of the basic 555 timer functions. They can also be used as a starting point to improve existing timer circuits or to develop new ones.

Miscellaneous Notes

Power Supply Bypassing: The original 555 Timer IC’s were made using a bipolar technology and required significant power supply bypassing (like early digital TTL ICs). Current spikes during output transitions could exceed 250mA. The CSS555C employs a “break-before-make” CMOS output driver that eliminates these spikes. Minimal supply bypassing is therefore required. A 0.001 uF capacitor is usually adequate for most applications. If a large capacitive load needs to be driven by the Timer Output, a larger bypass capacitor may be required.

Control Voltage: The Control Voltage input (pin 5) provides access to the upper level trip point. It is derived from a high impedance resistive divider. As with any high impedance node, it should be isolated from sources of DC leakage and high-level clock/data signals that might be capacitively coupled into it. Keep this trace as short as possible. When possible, surround (shield) the Control Voltage signal with an AC ground. In most applications it does not require a bypass capacitor.

Stray Capacitance: When using the CSS555C, it is important to minimize the stray capacitance on the Threshold and Discharge pins. The internal timing capacitor is 100pF. Printed circuit boards typically add several picofarads of stray capacitance if the routing is kept as short as possible. Timing resistors \( R_A \) and \( R_B \) should be located as close to the IC as possible. The stray capacitance (\( C_{STRAY} \)) will be fairly consistent from board-to-board and can be accounted for when selecting the timing resistors. (The internal timing capacitor can be electronically trimmed to adjust for variations in \( C_{STRAY} \), \( R_A \) and \( R_B \).) During development, remember that test sockets, proto-boards, connectors and cables can add significant stray capacitance to these nodes. (A typical proto-board adds about 5pF per pin.) In most prototype fixtures, the monostable delay times and astable periods will be longer than expected. After a PCB is built, delay times will approach their expected values.

Micro-power Monostable & Delay Functions

Micro-power One Shot

Standard 555 configuration

\[ t_{PW} = 1.1 \times (R_A + R_B) \times C_T \]

See Page 6

Long Range Delay Timer

Extended range – 1 msec to days

\[ t_{PW} = \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T \]

See Page 7
Micro-power Monostable & Delay Functions (continued)

One Shot with Internal \( C_T \)

No external timing capacitor, \( PW_{MAX} \sim 10 \text{ min.} \)

\[
t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

Low Voltage One Shot

\( V_{DD\text{MIN}} = 1.2\text{V}, \text{ trip levels} = 10\% \text{ & } 90\% \)

\[
t_{PW} = 2.3 \times (R_A+R_B) \times C_T \text{ (if Mult = 1)}
\]

\[
t_{PW} = \text{Multiplier} \times 2.2 \times (R_A+2R_B) \times C_T
\]

One Shot with Delay

Delay = Pulse Width

\[
t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

\[
t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

One Shot with Delay

Delay > Pulse Width

\[
t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A||R_F+2R_B) \times C_T
\]

\[
t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

One Shot with Delay

Delay >> Pulse Width

\[
t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

\[
t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

One Shot with Delay

Delay << Pulse Width

\[
t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]

\[
t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T
\]
Micro-power Astable Functions

Micro-power Clock Generator
Standard 555 configuration

Minimum Component Clock Generator
50% duty cycle

Low Frequency Clock Generator
50% duty cycle, internal counter

Low Voltage Clock Generator
50% duty cycle, 10% & 90% trip levels

Astable with Adjustable Duty Cycle
Duty Cycle = 1% to 50%

Astable with Adjustable Duty Cycle
Duty Cycle = 50% to 99%

Freq = 1.44 / \(|(R_A+2R_B) \times C_T|\)
Freq = 1.44 / \((2R_A \times C_T)\)
Freq = 1.44 / \([\text{Multiplier} \times (R_A+2R_B) \times C_T]\)
Freq = 0.455 / \([\text{Multiplier} \times (R_A+2R_B) \times C_T]\)

If \( R_B << R_A \) and \( R_F \):
Duty Cycle ~ \( R_F / (R_A+2R_F) \)
Duty Cycle ~ \( (R_A + R_F) / (R_A+2R_F) \)
### CSS555(C) Application Circuits

#### Applications with Special Requirements

**High Humidity/High Leakage Applications**

- **Low impedance Control Voltage**
  - 
  
  \[ V_{\text{CONTROL}} = V_{\text{DD}} \times R_{\text{DV2}} / (R_{\text{DV1}} + R_{\text{DV2}}) \]
  - For standard trip levels, \( R_{\text{DV2}} = 2 \times R_{\text{DV1}} \)

**Electronic Trimming**

- Trim the internal 100 pF timing capacitor

**Internal \( C_T \) Range ~ 85 pF to 115 pF**
- **Internal \( C_T \) Resolution ~ 1/8 pF**

### Isolated Power Supply

**Capacitor isolation**

- **Simple diode regulator**
  - (Low \( I_{\text{DD}} \) makes this practical with small cap’s.)

### High Voltage Power Supply

- **Typical Values**
  - \( C_C \) ~ 0.001 uF
  - \( C_T \) ~ 0.1 uF
  - \( C_{\text{DIV}} \) ~ used if \( V_{\text{IN}} > 6 \) V
  - Clock Freq ~ 32 KHz

- **LED acts as a Zener diode**

### Solar Powered Timer

**Micro-power circuit**

- **Typical Values**
  - \( C_C \) ~ 0.001 uF
  - \( C_T \) ~ 0.1 uF
  - Clock Freq ~ 32 KHz

- **Output** = 1 if no Reset pulse for > 1 minute

### 1 Minute Watch-dog Timer (also Missing Pulse Detector)

- **Using Astable delayed pulse circuit**

- **Output** = 1 if no Reset pulse for > 1 minute
Monostable & Delay Circuits
The following circuits use the CSS555 and CSS555C to implement micro-power delay timers.

Micro-power One Shot
This circuit uses the CSS555 configured to mimic the classic 555 timer, but with an operating current that is 10 times lower than any other 555 IC.

Design Example: Pulse Width ($t_{PW}$) = 1 second
Configuration Data (EEPROM):
  Multiplier = 1 (counter disabled), Mode = X (Don't Care)
  Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
  $R_A = 2.7\,\text{M}\Omega$, $R_B = 100\,\text{K}\Omega$, $C_T = 0.33\,\mu\text{F}$

Timing Equations:
Output Pulse Width ($t_{PW}$)
$$t_{PW} = 1.1 \times (R_A + R_B) \times C_T$$
$$= 1.1 \times (2.7\,\text{M}\Omega + 0.1\,\text{M}\Omega) \times 0.33\,\mu\text{F}$$
$$= 1.015\,\text{seconds}$$

Supply Current & Power:
Standby current ($I_{DD0}$) (Discharge = 0)
At $V_{DD} = 3.0\,\text{V}$, $I_{DD0} = 4.2\,\mu\text{A}$, Power = 12.6\,\mu\text{W}
At $V_{DD} = 5.0\,\text{V}$, $I_{DD0} = 6.1\,\mu\text{A}$, Power = 30.5\,\mu\text{W}
Average current ($I_{DD}$) (Output = 1)
At $V_{DD} = 3.0\,\text{V}$, $I_{DD} = 3.6\,\mu\text{A}$, Power = 10.8\,\mu\text{W}
At $V_{DD} = 5.0\,\text{V}$, $I_{DD} = 5.1\,\mu\text{A}$, Power = 25.5\,\mu\text{W}

Monostable Delay Time Examples

<table>
<thead>
<tr>
<th>Output Pulse Width</th>
<th>Timing Components</th>
<th>Supply Current ($I_{DD0}$)</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_A$</td>
<td>$R_B$</td>
<td>$C_T$</td>
</tr>
<tr>
<td>100 usec</td>
<td>0.5 MΩ</td>
<td>0.4 MΩ</td>
<td>100 pF</td>
</tr>
<tr>
<td>1 msec</td>
<td>2.7 MΩ</td>
<td>0.1 MΩ</td>
<td>330 pF</td>
</tr>
<tr>
<td>10 msec</td>
<td>2.7 MΩ</td>
<td>0.1 MΩ</td>
<td>33 nF</td>
</tr>
<tr>
<td>1 sec</td>
<td>2.7 MΩ</td>
<td>0.1 MΩ</td>
<td>0.33 uF</td>
</tr>
<tr>
<td>10 sec</td>
<td>2.7 MΩ</td>
<td>0.1 MΩ</td>
<td>3.3 uF</td>
</tr>
<tr>
<td>1 min</td>
<td>5.0 MΩ</td>
<td>0.5 MΩ</td>
<td>10 uF</td>
</tr>
</tbody>
</table>

Note: A calculator is available for this circuit. See file “CSS555_Timer_Delay_Calculator.xls”
CSS555(C)

Application Circuits

Monostable & Delay Circuits (continued)

Long Range Delay Timer

This circuit uses the CSS555’s internal counter to multiply (and therefore reduce) the value of the timing capacitor (C_T) by the counter setting (10 to 10^6). At the maximum counter setting, very long delay times are possible with small capacitor values.

**Design Example:** Pulse Width (t_PW) = 1 second

**Configuration Data (EEPROM):**
- Multiplier = 1000
- Mode = Monostable
- Power Setting = Micro
- Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- R_A = 2.4 MΩ
- R_B = 1.0 MΩ
- C_T = 330 pF

**Timing Equations:**
Output Pulse Width (t_PW)

\[
t_PW = \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T
\]

= 1000 \times 0.695 \times (2.4\,\text{MΩ} + 2 \times 1\,\text{MΩ}) \times 330\,\text{pF}

= 1.007\,\text{seconds}

**Supply Current & Power:**
- Standby current (I_DD0) (Discharge = 0)
  - At V_DD = 3.0V, I_DD0 = 4.4uA, Power = 13.2uW
  - At V_DD = 5.0V, I_DD0 = 6.4uA, Power = 32.0uW
- Average current (I_DD) (Output = 1)
  - At V_DD = 3.0V, I_DD = 3.5uA, Power = 10.5uW
  - At V_DD = 5.0V, I_DD = 4.8uA, Power = 24.0uW

**CSS555 Timer Calculator**

Note: A calculator is available for this circuit. See file “CSS555_Timer_Delay_Calculator.xls”

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### Monostable Delay Time Examples

<table>
<thead>
<tr>
<th>Output Pulse Width</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current (I_DD0)</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Multiplier</td>
<td>R_A</td>
<td>R_B</td>
</tr>
<tr>
<td>1 msec</td>
<td>10</td>
<td>240 KΩ</td>
<td>100 KΩ</td>
</tr>
<tr>
<td>10 msec</td>
<td>10</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>100 msec</td>
<td>100</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 sec</td>
<td>1K</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>10 sec</td>
<td>10K</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 min</td>
<td>100K</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>10 min</td>
<td>1M</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 hour</td>
<td>1M</td>
<td>2.4 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 day</td>
<td>1M</td>
<td>2.2 MΩ</td>
<td>1.0 MΩ</td>
</tr>
</tbody>
</table>
Monostable & Delay Circuits (continued)

One Shot with Minimal Components

This circuit uses the CSS555C’s internal counter and timing capacitor to eliminate the external capacitor.

**Design Example:** Pulse Width \( t_{PW} \) = 1 second

**Configuration Data (EEPROM):**
- Multiplier = 1000, Mode = Monostable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- \( R_A = 5.0 \, \text{M} \Omega \), \( R_B = 4.7 \, \text{M} \Omega \), \( C_T = 100 \, \text{pF} \)

**Timing Equations:**

\[
\begin{align*}
\text{Output Pulse Width} (t_{PW}) = & \quad \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T \\
= & \quad 1000 \times 0.695 \times (5.0 \, \text{M} \Omega + 2 \times 4.7 \, \text{M} \Omega) \times 100 \, \text{pF} \\
= & \quad 0.998 \text{ seconds}
\end{align*}
\]

**Supply Current & Power:**

- **Standby current** \( I_{DD0} \) (Discharge = 0)
  - At \( V_{DD} = 3.0 \, \text{V} \), \( I_{DD0} = 3.7 \, \mu \text{A} \), \( \text{Power} = 11.1 \, \mu \text{W} \)
  - At \( V_{DD} = 5.0 \, \text{V} \), \( I_{DD0} = 5.3 \, \mu \text{A} \), \( \text{Power} = 26.5 \, \mu \text{W} \)

- **Average current** \( I_{DD} \) (Output = 1)
  - At \( V_{DD} = 3.0 \, \text{V} \), \( I_{DD} = 3.2 \, \mu \text{A} \), \( \text{Power} = 9.6 \, \mu \text{W} \)
  - At \( V_{DD} = 5.0 \, \text{V} \), \( I_{DD} = 4.5 \, \mu \text{A} \), \( \text{Power} = 22.5 \, \mu \text{W} \)

**Monostable Delay Time Examples**

**Extended Period Mode & Internal Timing Capacitor**

<table>
<thead>
<tr>
<th>Output Pulse Width</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current ( I_{DD0} )</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Multiplier, ( R_A ), ( R_B ), ( C_T )</td>
<td>3.0V</td>
<td>5.0V</td>
</tr>
<tr>
<td>1 msec</td>
<td>10, 1.0 M( \Omega ), 200 K( \Omega ), 100 pF</td>
<td>6.1 ( \mu \text{A} )</td>
<td>9.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>10 msec</td>
<td>10, 5.0 M( \Omega ), 4.7 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>100 msec</td>
<td>100, 5.0 M( \Omega ), 4.7 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>1 sec</td>
<td>1K, 5.0 M( \Omega ), 4.7 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>10 sec</td>
<td>10K, 5.0 M( \Omega ), 4.7 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>1 min</td>
<td>100K, 5.0 M( \Omega ), 1.8 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
<tr>
<td>10 min</td>
<td>1M, 5.0 M( \Omega ), 1.8 M( \Omega ), 100 pF</td>
<td>3.7 ( \mu \text{A} )</td>
<td>5.3 ( \mu \text{A} )</td>
</tr>
</tbody>
</table>
Low Voltage One Shot
The trip levels are configured for 10% and 90% of \( V_{DD} \), allowing operation down to 1.2V. These trip levels may be used with or without the internal counter and timing capacitor.

**Design Example:** Pulse Width (\( t_{PW} \)) = 1 second

**Configuration Data (EEPROM):**
- Multiplier = 1000, Mode = Monostable
- Power Setting = Micro, Trip Levels = Low \( V_{DD} \) (10%, 90%)

**Timing Components:**
- \( R_A = 2.6 \, \text{M} \Omega \), \( R_B = 1.0 \, \text{M} \Omega \), \( C_T = 100 \, \text{pF} \)

**Timing Equations:**
Output Pulse Width (\( t_{PW} \))
\[
t_{PW} = \text{Multiplier} \times 2.197 \times (R_A + 2R_B) \times C_T
= 1000 \times 2.197 \times (2.6\, \text{M} \Omega + 2 \times 1.0\, \text{M} \Omega) \times 100 \, \text{pF}
= 1.01 \, \text{seconds}
\]

**Supply Current & Power:**
- Standby current (\( I_{DD0} \)) (Discharge = 0)
  - At \( V_{DD} = 1.5V \), \( I_{DD0} = 2.8uA \), Power = 4.2uW
  - At \( V_{DD} = 3.0V \), \( I_{DD0} = 4.3uA \), Power = 12.9uW
- Average current (\( I_{DD} \)) (Output = 1)
  - At \( V_{DD} = 1.5V \), \( I_{DD} = 2.4uA \), Power = 7.2uW
  - At \( V_{DD} = 3.0V \), \( I_{DD} = 3.5uA \), Power = 10.5uW

**Monostable Delay Time Examples**
Low \( V_{DD} \) Configuration (Trip levels = 10% & 90%)

<table>
<thead>
<tr>
<th>Output Pulse Width</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current (( I_{DD0} ))</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Multiplier</td>
<td>( R_A )</td>
<td>( R_B )</td>
</tr>
<tr>
<td>1 msec</td>
<td>1</td>
<td>3.3 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>10 msec</td>
<td>10</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>100 msec</td>
<td>100</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 sec</td>
<td>1K</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>10 sec</td>
<td>10K</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>1 min</td>
<td>100K</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>10 min</td>
<td>1M</td>
<td>2.6 MΩ</td>
<td>1.0 MΩ</td>
</tr>
</tbody>
</table>

Note: A calculator is available for this circuit. See file “CSS555_Timer_Delay_Calculator.xls”
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse

This circuit uses the CSS555’s internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first half of the counter cycle and high for the second half. The output pulse is therefore delayed by Mult/2 clock cycles and has a pulse width of Mult/2 cycles. This circuit can be used with or without the internal timing capacitor and Low \( V_{DD} \) trip levels.

**Design Example:** Delay \( (t_D) = 0.5 \text{ sec} \), Pulse Width \( (t_{PW}) = 0.5 \text{ sec} \)

**Configuration Data (EEPROM):**
- Multiplier = 1000 (for 0.5 second \( t_D \) & \( t_{PW} \)), Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components (for 0.5 sec pulse width & delay):**
- \( R_A = 5.0 \text{ M}\Omega \)
- \( R_B = 4.7 \text{ M}\Omega \)
- \( C_T = 100 \text{ pF} \)

**Timing Equations:**

Output Pulse Width & Delay \( (t_{PW}, t_D) \):
\[
t_{PW} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T
\]
\[
= 500 \times 0.695 \times (5.0\text{M}\Omega + 2\times4.7\text{M}\Omega) \times 100\text{pF}
\]
\[
= 0.499 \text{ seconds}
\]

\( t_D = t_{PW} = 0.499 \text{ seconds} \)

**Supply Current & Power:**

Standby current \( (I_{DD0}) \) (Discharge = 0):
- At \( V_{DD} = 3.0V \), \( I_{DD0} = 3.7\mu A \), Power = 11.1\text{uW}
- At \( V_{DD} = 5.0V \), \( I_{DD0} = 5.3\mu A \), Power = 26.5\text{uW}

Average current \( (I_{DD}) \) (Output = 1):
- At \( V_{DD} = 3.0V \), \( I_{DD} = 3.2\mu A \), Power = 9.6\text{uW}
- At \( V_{DD} = 5.0V \), \( I_{DD} = 4.5\mu A \), Power = 22.5\text{uW}

**Delayed-Pulse Examples**

<table>
<thead>
<tr>
<th>Output ( t_{D} + t_{PW} )</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current ( (I_{DD0}) )</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{D} + t_{PW} )</td>
<td>Multiplier</td>
<td>( R_A )</td>
<td>( R_B )</td>
</tr>
<tr>
<td>1 msec</td>
<td>10</td>
<td>1.0 MΩ</td>
<td>200 KΩ</td>
</tr>
<tr>
<td>10 msec</td>
<td>10</td>
<td>5.0 MΩ</td>
<td>4.7 MΩ</td>
</tr>
<tr>
<td>100 msec</td>
<td>100</td>
<td>5.0 MΩ</td>
<td>4.7 MΩ</td>
</tr>
<tr>
<td>1 sec</td>
<td>1K</td>
<td>5.0 MΩ</td>
<td>4.7 MΩ</td>
</tr>
<tr>
<td>10 sec</td>
<td>10K</td>
<td>5.0 MΩ</td>
<td>4.7 MΩ</td>
</tr>
<tr>
<td>1 min</td>
<td>100K</td>
<td>5.0 MΩ</td>
<td>1.8 MΩ</td>
</tr>
<tr>
<td>10 min</td>
<td>1M</td>
<td>5.0 MΩ</td>
<td>1.8 MΩ</td>
</tr>
</tbody>
</table>
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse (T_D > T_PW)

This circuit uses the CSS555’s internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first Mult/2 clock cycles and high for the remaining Mult/2 cycles. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the pulse width to be reduced. This circuit can be used with or without the internal timing capacitor.

**Design Example:** Delay (T_D) = 0.66 sec, Pulse Width (T_PW) = 0.33 sec

**Configuration Data (EEPROM):**
- Multiplier = 10K, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- R_A = 1.0 MΩ, R_B = 90 KΩ, R_F = 3.8 MΩ, C_T = 100 pF

**Timing Equations:**

Output Delay & Pulse Width (T_D, T_PW)

\[
T_D = \frac{1}{2} \times \text{Multiplier} \times C_T \times 0.693 \times (R_A|R_F+2R_B) \\
T_PW = \frac{1}{2} \times \text{Multiplier} \times C_T \times 0.693 \times (R_A|R_F+R_B) \\
\]

**Supply Current & Power:**

Maximum current (I_DD0) (Discharge = 0)
- At V_DD = 3.0V, I_DD0 = 4.7uA, Power = 11.1uW
- At V_DD = 5.0V, I_DD0 = 6.5uA, Power = 26.5uW

**Delayed-Pulse Examples (T_D > T_PW)**

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>R_A</th>
<th>R_B</th>
<th>R_F</th>
<th>C_T</th>
<th>Delay</th>
<th>Pulse Width</th>
<th>3.0V</th>
<th>5.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1K</td>
<td>1.0 MΩ</td>
<td>100 KΩ</td>
<td>5.0 MΩ</td>
<td>100 pF</td>
<td>59.6 msec</td>
<td>35.8 msec</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>1K</td>
<td>1.0 MΩ</td>
<td>100 KΩ</td>
<td>2.5 MΩ</td>
<td>100 pF</td>
<td>97.2 msec</td>
<td>31.7 msec</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>1K</td>
<td>1.0 MΩ</td>
<td>250 KΩ</td>
<td>2.5 MΩ</td>
<td>100 pF</td>
<td>119.7 msec</td>
<td>42.1 msec</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
</tbody>
</table>

Note: A calculator is available for this circuit. See file “CSS555_Adj_Duty_Calculator.xls”
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse \((t_D >> t_{PW})\)

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first \(\text{Mult}/2\) clock cycles and high for the remaining \(\text{Mult}/2\) cycles. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the pulse width to be reduced. This circuit can be used with or without the internal timing capacitor.

**Design Example:** Delay \((t_D) = 0.8\) sec, Pulse Width \((t_{PW}) = 0.2\) sec

Configuration Data (EEPROM):

- Multiplier = 10K, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

Timing Components:

- \(R_A = 2.1\) M\(\Omega\)
- \(R_B = 100\) K\(\Omega\)
- \(R_F = 380\) K\(\Omega\)
- \(C_T = 100\) pF

Timing Equations:

- Output Delay & Pulse Width \((t_D, t_{PW})\)
  \[
  t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T \\
  \quad = 5000 \times 0.695 \times (2.1\text{M}\Omega + 2\times0.1\text{M}\Omega) \times 100\text{pF} \\
  \quad = 799\text{msec}
  \\
  t_{PW} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A|R_F+2R_B) \times C_T \\
  \quad = 5000 \times 0.695 \times (0.32\text{M}\Omega + 2\times0.1\text{M}\Omega) \times 100\text{pF} \\
  \quad = 181\text{msec (if ideal diode)} \\
  \quad \sim 198\text{msec (adding diode voltage drop)}
  \]

Supply Current & Power:

- Maximum current \((I_{DD0})\) (Discharge = 0)
  - At \(V_{DD} = 3.0\) V, \(I_{DD0} = 4.7\) uA, Power = 11.1 uW
  - At \(V_{DD} = 5.0\) V, \(I_{DD0} = 6.5\) uA, Power = 26.5 uW

Delayed-Pulse Examples \((t_D >> t_{PW})\)

**Astable Mode, Delay \((t_D) >>\) Pulse Width \((t_{PW})\)**

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>(R_A)</th>
<th>(R_B)</th>
<th>(R_F)</th>
<th>(C_T)</th>
<th>Delay</th>
<th>Pulse Width</th>
<th>(3.0) V</th>
<th>(5.0) V</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 pF</td>
<td>416 usec</td>
<td>106 usec</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>10</td>
<td>5.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 pF</td>
<td>1.80 msec</td>
<td>0.11 msec</td>
<td>3.9 uA</td>
<td>5.1 uA</td>
</tr>
<tr>
<td>10</td>
<td>5.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>5.0 M(\Omega)</td>
<td>100 pF</td>
<td>1.80 msec</td>
<td>1.01 msec</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
<tr>
<td>10K</td>
<td>1.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 pF</td>
<td>416 msec</td>
<td>106 msec</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>10K</td>
<td>5.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 K(\Omega)</td>
<td>100 pF</td>
<td>1.80 sec</td>
<td>0.11 sec</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
<tr>
<td>10K</td>
<td>5.0 M(\Omega)</td>
<td>100 K(\Omega)</td>
<td>5.0 M(\Omega)</td>
<td>100 pF</td>
<td>1.80 sec</td>
<td>1.01 sec</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
</tbody>
</table>

Note: A calculator is available for this circuit. See file “CSS555_Adj_Duty_Calculator.xls”
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse ($t_D << t_{PW}$)

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first $\text{Mult}/2$ clock cycles and high for the remaining $\text{Mult}/2$ cycles. Feedback from the Timer Output increases the oscillator frequency when the output is low, allowing the delay to be reduced. This circuit can be used with or without the internal timing capacitor.

**Design Example:** Delay ($t_D$) = 0.2 sec, Pulse Width ($t_{PW}$) = 0.8 sec

**Configuration Data (EEPROM):**
- Multiplier = 10K, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- $R_A = 2.1 \text{ M}\Omega$, $R_B = 100 \text{ K}\Omega$, $R_F = 460 \text{ K}\Omega$, $C_T = 100 \text{ pF}$

**Timing Equations:**

Output Delay & Pulse Width ($t_D$, $t_{PW}$)

$$t_D = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A || R_F + 2R_B) \times C_T$$

$$t_{PW} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T$$

$$= 5000 \times 0.695 \times (0.377\text{M}\Omega + 2 \times 0.1\text{M}\Omega) \times 100\text{pF}$$

$$= 200 \text{ msec}$$

$$= 5000 \times 0.695 \times (2.1\text{M}\Omega + 2 \times 0.1\text{M}\Omega) \times 100\text{pF}$$

$$= 799 \text{ msec}$$

**Supply Current & Power:**

Maximum current ($I_{DD0}$) (Discharge = 0)

- At $V_{DD} = 3.0\text{V}$, $I_{DD0} = 4.7\text{uA}$, Power = 11.1uW
- At $V_{DD} = 5.0\text{V}$, $I_{DD0} = 6.5\text{uA}$, Power = 26.5uW

**Delayed-Pulse Examples ($t_D >> t_{PW}$)**

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>$R_A$</th>
<th>$R_B$</th>
<th>$R_F$</th>
<th>$C_T$</th>
<th>Delay (usec)</th>
<th>Pulse Width (usec)</th>
<th>$I_{DD0}$ (3.0V)</th>
<th>$I_{DD0}$ (5.0V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.0 MΩ</td>
<td>100 KΩ</td>
<td>100 KΩ</td>
<td>100 pF</td>
<td>416</td>
<td>106</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>10</td>
<td>5.0 MΩ</td>
<td>100 KΩ</td>
<td>100 KΩ</td>
<td>100 pF</td>
<td>1.80</td>
<td>0.11</td>
<td>3.9 uA</td>
<td>5.1 uA</td>
</tr>
<tr>
<td>10</td>
<td>5.0 MΩ</td>
<td>100 KΩ</td>
<td>5.0 MΩ</td>
<td>100 pF</td>
<td>1.80</td>
<td>1.01</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
<tr>
<td>10K</td>
<td>1.0 MΩ</td>
<td>100 KΩ</td>
<td>100 KΩ</td>
<td>200 pF</td>
<td>416</td>
<td>106</td>
<td>6.3 uA</td>
<td>9.1 uA</td>
</tr>
<tr>
<td>10K</td>
<td>5.0 MΩ</td>
<td>100 KΩ</td>
<td>100 KΩ</td>
<td>100 pF</td>
<td>1.80</td>
<td>0.11</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
<tr>
<td>10K</td>
<td>5.0 MΩ</td>
<td>100 KΩ</td>
<td>5.0 MΩ</td>
<td>100 pF</td>
<td>1.80</td>
<td>1.01</td>
<td>3.7 uA</td>
<td>5.3 uA</td>
</tr>
</tbody>
</table>
Astable Circuits
The following circuits use the CSS555 and CSS555C to implement micro-power astable timers.

Micro-power Clock Generator
This circuit uses the CSS555 configured to mimic the classic 555 Timer, but with an operating current that is 10 times lower than all other 555 ICs.

Design Example: Output Frequency \( (F_{\text{OUT}}) = 100 \text{ Hz} \)
Configuration Data (EEPROM):
- Multiplier = 1 (counter disabled), Mode = X (Don’t Care)
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
- \( R_A = 2.0 \text{ M}\Omega \), \( R_B = 1.2 \text{ M}\Omega \), \( C_T = 3.3 \text{ nF} \)

Timing Equations:
- Output Period & Frequency \( (t_{\text{PER}}, F_{\text{OUT}}) \)
  \[ t_{\text{PER}} = 0.695 \times (R_A+2R_B) \times C_T \]
  \[ F_{\text{OUT}} = 1.44 / [(R_A+2R_B) \times C_T] \]
  \[ = 1.44 / [(2.0\text{M}\Omega + 2 \times 1.2\text{M}\Omega) \times 3.3\text{nF}] \]
  \[ = 99.2 \text{ Hz} \]
Duty Cycle = \( R_B / (R_A+2R_B) \)

Supply Current & Power:
- Standby current \( (I_{\text{DD0}}) (\text{Discharge} = 0) \)
  - At \( V_{\text{DD}} = 3.0V \), \( I_{\text{DD0}} = 4.6uA \), Power = 13.8uW
  - At \( V_{\text{DD}} = 5.0V \), \( I_{\text{DD0}} = 6.8uA \), Power = 34.0uW
Average current \( (I_{\text{DD}}) (\text{Output toggling}) \)
  - At \( V_{\text{DD}} = 3.0V \), \( I_{\text{DD}} = 3.5uA \), Power = 10.5uW
  - At \( V_{\text{DD}} = 5.0V \), \( I_{\text{DD}} = 4.8uA \), Power = 24.0uW

CSS555 Timer Calculator
Note: A calculator is available for this circuit. See file “CSS555_Timer_Delay_Calculator.xls”

Micro-power Astable Examples

<table>
<thead>
<tr>
<th>Output Frequency</th>
<th>Timing Components</th>
<th>Supply Current ( (I_{\text{DD}}) )</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( R_A )</td>
<td>( R_B )</td>
<td>( C_T )</td>
</tr>
<tr>
<td>100 KHz</td>
<td>70 K\Omega</td>
<td>37 K\Omega</td>
<td>100 pF</td>
</tr>
<tr>
<td>10 KHz</td>
<td>700 K\Omega</td>
<td>370 K\Omega</td>
<td>100 pF</td>
</tr>
<tr>
<td>1 KHz</td>
<td>2.0 M\Omega</td>
<td>1.2 M\Omega</td>
<td>330 pF</td>
</tr>
<tr>
<td>100 Hz</td>
<td>2.0 M\Omega</td>
<td>1.2 M\Omega</td>
<td>3.3 nF</td>
</tr>
<tr>
<td>10 Hz</td>
<td>2.0 M\Omega</td>
<td>1.2 M\Omega</td>
<td>0.033 uF</td>
</tr>
<tr>
<td>1 Hz</td>
<td>2.0 M\Omega</td>
<td>1.2 M\Omega</td>
<td>0.33 uF</td>
</tr>
</tbody>
</table>
Astable Circuits (continued)

Micro-power Clock Generator (minimum component)
This circuit uses the CSS555 configured to mimic the classic 555 Timer, but with an operating current that is 10 times lower than all other 555 ICs. It requires just one timing resistor and has a 50% duty cycle. This circuit can be used with or without the internal timing capacitor.

Design Example: Output Frequency \(F_{OUT} = 100 \text{ Hz}\)
Configuration Data (EEPROM):
    - Multiplier = 1 (counter disabled), Mode = X (Don’t Care)
    - Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
    - \(R_A = 2.2 \text{ MΩ}, C_T = 3.3 \text{ nF}\)

Timing Equations:
Output Period & Frequency \(t_{PER}, F_{OUT}\)
\[t_{PER} = 0.695 \times 2R_A \times C_T\]
\[F_{OUT} = 1.44 / (2R_A \times C_T)\]
\[= 1.44 / (2 \times 2.2 \text{ MΩ} \times 3.3 \text{ nF})\]
\[= 99.2 \text{ Hz}\]
Duty Cycle = 50%

Supply Current & Power:
Standby current \((I_{DD0})(\text{Reset = 0})\)
At \(V_{DD} = 3.0\text{V}, I_{DD0} = 3.1\mu\text{A}, \text{Power} = 9.3\mu\text{W}\)
At \(V_{DD} = 5.0\text{V}, I_{DD0} = 4.3\mu\text{A}, \text{Power} = 21.5\mu\text{W}\)
Average current \((I_{DD})(\text{Output toggling})\)
At \(V_{DD} = 3.0\text{V}, I_{DD} = 3.5\mu\text{A}, \text{Power} = 10.5\mu\text{W}\)
At \(V_{DD} = 5.0\text{V}, I_{DD} = 4.8\mu\text{A}, \text{Power} = 24.0\mu\text{W}\)

Minimal Component Astable Examples

<table>
<thead>
<tr>
<th>Output Frequency</th>
<th>Timing Components</th>
<th>Supply Current ((I_{DD}))</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(R_A)</td>
<td>(R_B)</td>
<td>(C_T)</td>
</tr>
<tr>
<td>100 KHz</td>
<td>70 KΩ</td>
<td>100 pF</td>
<td>13.4 \mu A, 21.5 \mu A</td>
</tr>
<tr>
<td>10 KHz</td>
<td>700 KΩ</td>
<td>100 pF</td>
<td>4.2 \mu A, 6.0 \mu A</td>
</tr>
<tr>
<td>1 KHz</td>
<td>2.2 MΩ</td>
<td>330 pF</td>
<td>3.5 \mu A, 4.8 \mu A</td>
</tr>
<tr>
<td>100 Hz</td>
<td>2.2 MΩ</td>
<td>3.3 nF</td>
<td>3.5 \mu A, 4.8 \mu A</td>
</tr>
<tr>
<td>10 Hz</td>
<td>2.2 MΩ</td>
<td>0.033 \mu F</td>
<td>3.5 \mu A, 4.8 \mu A</td>
</tr>
<tr>
<td>1 Hz</td>
<td>2.2 MΩ</td>
<td>0.33 \mu F</td>
<td>3.5 \mu A, 4.8 \mu A</td>
</tr>
</tbody>
</table>
Astable Circuits (continued)

Low Frequency Clock Generator
This circuit uses the CSS555’s internal counter to multiply (and therefore reduce) the value of the timing capacitor (CT) by the counter setting (10 to 106). At the maximum counter setting, very low frequency clocks are possible with small capacitor values. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

Design Example: Output Frequency (FOUT) = 1.0 Hz
Configuration Data (EEPROM):
- Multiplier = 1000, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
- RA = 5.0 MΩ, RB = 4.7 MΩ, CT = 100 pF

Timing Equations:
- Output Period & Frequency (tPER, FOUT)
  \[ t_{\text{PER}} = \text{Multiplier} \times 0.695 \times \left( R_A + 2R_B \right) \times C_T \]
  \[ F_{\text{OUT}} = \frac{1.44}{[\text{Multiplier} \times (R_A+2R_B) \times C_T]} \]
  \[ = \frac{1.44}{[1000 \times (5.0 M\Omega + 2 \times 4.7 M\Omega) \times 100 pF]} \]
  \[ = 1.00 Hz \]
- Duty Cycle = 50%

Supply Current & Power:
- Standby current (IDD0) (Discharge = 0)
  - At VDD = 3.0V, IDD0 = 3.7uA, Power = 11.1uW
  - At VDD = 5.0V, IDD0 = 5.3uA, Power = 26.5uW
- Average current (IDD) (Output toggling)
  - At VDD = 3.0V, IDD = 3.2uA, Power = 9.6uW
  - At VDD = 5.0V, IDD = 4.5uA, Power = 22.5uW

Low Frequency Astable Examples

<table>
<thead>
<tr>
<th>Output Frequency</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current (IDD0)</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Multiplier</td>
<td>RA (MΩ)</td>
<td>RB (MΩ)</td>
</tr>
<tr>
<td>10 KHz</td>
<td>1</td>
<td>500</td>
<td>470</td>
</tr>
<tr>
<td>1K Hz</td>
<td>1</td>
<td>5.0</td>
<td>4.7</td>
</tr>
<tr>
<td>100 Hz</td>
<td>10</td>
<td>5.0</td>
<td>4.7</td>
</tr>
<tr>
<td>10 Hz</td>
<td>100</td>
<td>5.0</td>
<td>4.7</td>
</tr>
<tr>
<td>1 Hz</td>
<td>1000</td>
<td>5.0</td>
<td>4.7</td>
</tr>
</tbody>
</table>
Astable Circuits (continued)

Low Voltage Clock Generator
The trip levels are configured for 10% and 90% of \( V_{DD} \), allowing operation down to 1.2V. The TRIGGER input acts as a gate for the clock. These trip levels may be used with or without the internal counter and timing capacitor.

**Design Example:** Output Frequency \( (F_{OUT}) = 60 \text{ Hz} \)

**Configuration Data (EEPROM):**
- Multiplier = 10, Mode = Astable
- Power Setting = Micro, Trip Levels = Low \( V_{DD} \) (10%, 90%)

**Timing Components:**
- \( R_A = 2.5 \text{ M}\Omega \)
- \( R_B = 2.5 \text{ M}\Omega \)
- \( C_T = 100 \text{ pF} \)

**Timing Equations:**
- Output Period & Frequency \( (t_{PER}, F_{OUT}) \)
  \[
  t_{PER} = \text{Multiplier} \times 2.197 \times (R_A + 2R_B) \times C_T
  \]
  \[
  F_{OUT} = \frac{0.455}{\text{Multiplier} \times (R_A + 2R_B) \times C_T}
  \]
  \[
  = \frac{0.455}{10 (2.5\text{M}\Omega + 2 \times 2.5\text{M}\Omega) \times 100\text{pF}}
  \]
  \[
  = 60.7 \text{ Hz}
  \]
- Duty Cycle = 50%

**Supply Current & Power:**
- **Standby current \( (I_{DDD}) \) (Discharge = 0)**
  - At \( V_{DD} = 1.5V \), \( I_{DDD} = 2.9\text{uA} \), Power = 4.4\text{uW}  
  - At \( V_{DD} = 3.0V \), \( I_{DDD} = 4.3\text{uA} \), Power = 12.9\text{uW}
- **Average current \( (I_{DD}) \) (Output toggling)**
  - At \( V_{DD} = 1.5V \), \( I_{DD} = 2.3\text{uA} \), Power = 3.5\text{uW} 
  - At \( V_{DD} = 3.0V \), \( I_{DD} = 3.3\text{uA} \), Power = 9.9\text{uW}

**Low Voltage Astable Examples**

<table>
<thead>
<tr>
<th>Output Frequency</th>
<th>Configuration Data &amp; Timing Components</th>
<th>Supply Current ( (I_{DDD}) )</th>
<th>Supply Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Multiplier, ( R_A ), ( R_B ), ( C_T )</td>
<td>1.5V</td>
<td>3.0V</td>
</tr>
<tr>
<td>10 KHz</td>
<td>1, 200 \text{K}\Omega, 120 \text{K}\Omega, 100 \text{pF}</td>
<td>9.8 \text{uA}</td>
<td>18.1 \text{uA}</td>
</tr>
<tr>
<td>1K Hz</td>
<td>1, 2.0 \text{M}\Omega, 1.2 \text{M}\Omega, 100 \text{pF}</td>
<td>3.0 \text{uA}</td>
<td>4.6 \text{uA}</td>
</tr>
<tr>
<td>100 Hz</td>
<td>10, 2.0 \text{M}\Omega, 1.2 \text{M}\Omega, 100 \text{pF}</td>
<td>3.0 \text{uA}</td>
<td>4.6 \text{uA}</td>
</tr>
<tr>
<td>10 Hz</td>
<td>100, 2.0 \text{M}\Omega, 1.2 \text{M}\Omega, 100 \text{pF}</td>
<td>3.0 \text{uA}</td>
<td>4.6 \text{uA}</td>
</tr>
<tr>
<td>1 Hz</td>
<td>1000, 2.0 \text{M}\Omega, 1.2 \text{M}\Omega, 100 \text{pF}</td>
<td>3.0 \text{uA}</td>
<td>4.6 \text{uA}</td>
</tr>
</tbody>
</table>
Astable Circuits (continued)

Astable with Adjustable Duty Cycle (Duty cycle = 1% to 50%)
This circuit uses the CSS555's internal counter and astable operating mode to generate a continuous clock. In the astable mode, the timer output is derived from the MSB of the counter. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the duty cycle to be reduced. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

**Design Example:**
Output Frequency \( (F_{OUT}) = 100 \text{ Hz} \)

**Configuration Data (EEPROM):**
- Multiplier = 100, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- \( R_A = 2.1 \text{ M}\Omega \)
- \( R_B = 150 \text{ K}\Omega \)
- \( R_F = 150 \text{ K}\Omega \)
- \( C_T = 100 \text{ pF} \)

**Timing Equations:**
- Output Period & Frequency \( (t_{PER}, F_{OUT}) \)
  - \( t_{DL} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T \)
  - \( = 50 \times 0.695 \times (2.1\text{M}\Omega + 2 \times 0.15\text{M}\Omega) \times 100\text{pF} \)
  - \( = 8.34 \text{ msec} \)
  - \( t_{DH} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A||R_F + 2R_B) \times C_T \)
  - \( = 50 \times 0.695 \times (140\text{K}\Omega + 2 \times 150\text{K}\Omega) \times 100\text{pF} \)
  - \( = 1.53 \text{ msec (if ideal diode)} \)
  - \( \sim 1.69 \text{ msec (adding diode voltage drop)} \)
- \( t_{PER} = (t_{DL} + t_{DH}) = 8.34 + 1.69 = 10.03 \text{ msec} \)
- \( F_{OUT} = 1 / t_{PER} = 1/10.03 \text{ msec} = 99.7 \text{ Hz} \)
- Duty Cycle = \( (t_{DH} / t_{PER}) = 1.69/10.03 = 16.8\% \)

**Supply Current & Power:**
- Maximum current (\( I_{DD0} \)) (Discharge = 0)
  - At \( V_{DD} = 3.0\text{V} \), \( I_{DD0} = 4.3\mu\text{A} \), Power = 12.9\mu\text{W} 
  - At \( V_{DD} = 5.0\text{V} \), \( I_{DD0} = 5.8\mu\text{A} \), Power = 29.0\mu\text{W} 

**Astable with Adjustable Duty Cycle Examples (Duty Cycle < 50%)**

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>( R_A )</th>
<th>( R_B )</th>
<th>( R_F )</th>
<th>( C_T )</th>
<th>Frequency</th>
<th>Duty Cycle</th>
<th>( I_{DD0} ) (3.0V)</th>
<th>( I_{DD0} ) (5.0V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ pF}</td>
<td>1898 Hz</td>
<td>21.1%</td>
<td>6.3 \mu\text{A}</td>
<td>9.1 \mu\text{A}</td>
</tr>
<tr>
<td>10</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ pF}</td>
<td>522 Hz</td>
<td>6.0%</td>
<td>3.9 \mu\text{A}</td>
<td>5.1 \mu\text{A}</td>
</tr>
<tr>
<td>10</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ pF}</td>
<td>348 Hz</td>
<td>37.2%</td>
<td>3.9 \mu\text{A}</td>
<td>5.1 \mu\text{A}</td>
</tr>
<tr>
<td>100</td>
<td>1.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ pF}</td>
<td>190 Hz</td>
<td>21.1%</td>
<td>6.3 \mu\text{A}</td>
<td>9.1 \mu\text{A}</td>
</tr>
<tr>
<td>100</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>100 \text{ pF}</td>
<td>52.2 Hz</td>
<td>6.0%</td>
<td>3.9 \mu\text{A}</td>
<td>5.1 \mu\text{A}</td>
</tr>
<tr>
<td>100</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ K}\Omega</td>
<td>5.0 \text{ M}\Omega</td>
<td>100 \text{ pF}</td>
<td>34.8 Hz</td>
<td>37.2%</td>
<td>3.9 \mu\text{A}</td>
<td>5.1 \mu\text{A}</td>
</tr>
</tbody>
</table>
Astable Circuits (continued)

Astable with Adjustable Duty Cycle (Duty cycle = 50% to 99%)

This circuit uses the CSS555’s internal counter and astable operating mode to generate a continuous clock. In the astable mode, the timer output is derived from the MSB of the counter. Feedback from the Timer Output increases the oscillator frequency when the output is low, allowing the duty cycle to be raised. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

**Design Example:** Output Frequency ($F_{OUT}$) = 100 Hz

**Configuration Data (EEPROM):**
- Multiplier = 100, Mode = Astable
- Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)

**Timing Components:**
- $R_A = 2.1 \, \text{M}\Omega$, $R_B = 150 \, \text{K}\Omega$, $R_F = 150 \, \text{K}\Omega$, $C_T = 100 \, \text{pF}$

**Timing Equations:**
- Output Period & Frequency ($t_{PER}$, $F_{OUT}$)
  - $t_{DL} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A || R_F + 2R_B) \times C_T$
  - $= 50 \times 0.695 \times (140 \, \text{K}\Omega + 2 \times 150 \, \text{K}\Omega) \times 100 \, \text{pF}$
  - $= 1.52 \, \text{msec}$
  - $t_{DH} = 0.5 \times \text{Multiplier} \times 0.695 \times (R_A + 2R_B) \times C_T$
  - $= 50 \times 0.695 \times (2.1 \, \text{M}\Omega + 2 \times 0.15 \, \text{M}\Omega) \times 100 \, \text{pF}$
  - $= 8.32 \, \text{msec}$
  - $t_{PER} = (t_{DL} + t_{DH}) = 1.52 + 8.32 = 9.84 \, \text{msec}$
  - $F_{OUT} = 1 / t_{PER} = 1 / 9.84 \, \text{msec} = 101.6 \, \text{Hz}$
  - Duty Cycle = $(t_{DH} / t_{PER}) = 8.32 / 9.84 = 84.5\%$

**Supply Current & Power:**
- Maximum current ($I_{DD0}$) (Discharge = 0)
  - At $V_{DD} = 3.0\, \text{V}$, $I_{DD0} = 4.7\, \text{uA}$, Power = 14.1\,\text{uW}$
  - At $V_{DD} = 5.0\, \text{V}$, $I_{DD0} = 6.5\, \text{uA}$, Power = 32.5\,\text{uW}$

### Astable with Adjustable Duty Cycle Examples (Duty Cycle > 50%)  

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>$R_A$</th>
<th>$R_B$</th>
<th>$R_F$</th>
<th>$C_T$</th>
<th>Frequency</th>
<th>Duty Cycle</th>
<th>$I_{DD0}$ (3.0,\text{V})</th>
<th>$I_{DD0}$ (5.0,\text{V})</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{pF}</td>
<td>1935 ,\text{Hz}</td>
<td>80.5%</td>
<td>6.3 ,\text{uA}</td>
<td>9.1 ,\text{uA}</td>
</tr>
<tr>
<td>10</td>
<td>5.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{pF}</td>
<td>525 ,\text{Hz}</td>
<td>94.6%</td>
<td>3.9 ,\text{uA}</td>
<td>5.1 ,\text{uA}</td>
</tr>
<tr>
<td>10</td>
<td>5.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>5.0 , \text{M}\Omega</td>
<td>100 , \text{pF}</td>
<td>365 ,\text{Hz}</td>
<td>65.8%</td>
<td>3.9 ,\text{uA}</td>
<td>5.1 ,\text{uA}</td>
</tr>
<tr>
<td>100</td>
<td>1.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{pF}</td>
<td>193 ,\text{Hz}</td>
<td>80.5%</td>
<td>6.3 ,\text{uA}</td>
<td>9.1 ,\text{uA}</td>
</tr>
<tr>
<td>100</td>
<td>5.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>100 , \text{pF}</td>
<td>525 ,\text{Hz}</td>
<td>94.6%</td>
<td>3.9 ,\text{uA}</td>
<td>5.1 ,\text{uA}</td>
</tr>
<tr>
<td>100</td>
<td>5.0,\text{M}\Omega</td>
<td>100 , \text{K}\Omega</td>
<td>5.0 , \text{M}\Omega</td>
<td>100 , \text{pF}</td>
<td>36.5 ,\text{Hz}</td>
<td>65.8%</td>
<td>3.9 ,\text{uA}</td>
<td>5.1 ,\text{uA}</td>
</tr>
</tbody>
</table>
Applications with Special Requirements

Capacitor Isolated Power Supply

In applications that require an isolated power supply, a simple charge pump can provide a very efficient, capacitively coupled supply. The exceptionally low supply current of the CSS555 allows the values of the coupling and filter capacitors (C_C & C_F) to be very small (and low cost). Adding a third capacitor (C_DIV) attenuates the amplitude of the input clock, allowing this circuit to be used with high voltage AC supplies.

**Design Example 1:**

\[
V_{\text{IN}} = 3\text{V Square wave or pulse:} \quad \text{Freq} \ (F_{\text{CLK}}) = 32 \text{KHz, Amplitude} \ (V_{p-p}) = 3.0\text{V}
\]

Charge Pump Components:

\[
C_C = 0.001 \text{ uF,} \quad C_F = 0.033 \text{ uF}
\]

\[
D_1, D_2 = 1\text{N914}
\]

**Design Example 2:**

\[
V_{\text{IN}} = 24\text{V RMS Sine wave:} \quad \text{Freq} \ (F_{\text{CLK}}) = 60 \text{Hz, Amplitude} \ (V_{p-p}) = 67.9\text{V}
\]

Charge Pump Components:

\[
C_C = 0.033 \text{ uF,} \quad C_F = 10 \text{ uF}
\]

\[
C_{\text{DIV}} = 0.47\text{uF,} \quad D_1, D_2 = 1\text{N914}
\]

**Design Equations:**

Thevenin equivalent voltage source:

\[
V_{OC} = V_{\text{IN}} - (2 \times V_D) \quad (V_D = \text{diode} \ V_{\text{ON}})
\]

\[
= 3.0 - (2 \times 0.4) = 2.2\text{V}
\]

\[
I_{SC} = F_{\text{CLK}} \times V_{OC} \times C_C
\]

\[
= 32K \times 2.2 \times 0.001 = 70.4\text{uA}
\]

\[
R_{\text{THV}} = \frac{V_{OC}}{I_{SC}} = 31.3 \text{K}\Omega
\]

If \(R_{\text{LOAD}} = 500\text{K}\Omega:

\[
V_{\text{DD}} = \frac{V_{OC} \times R_{\text{LOAD}}}{(R_{\text{LOAD}} + R_{\text{THV}})}
\]

\[
= 2.2 \times 500K / (500K + 31.3K) = 2.07\text{V}
\]

Output Ripple Voltage (\(V_{\text{RIP}}\)):

\[
V_{\text{RIP}} = I_{\text{DD}} / (F_{\text{CLK}} \times C_F)
\]

\[
= V_{\text{DD}} / (R_{\text{LOAD}} \times F_{\text{CLK}} \times C_F)
\]

\[
= 2.07 / (500K \times 32K \times 0.033) = 3.9mV
\]

Output Ripple Voltage (\(V_{\text{RIP}}\)):

\[
V_{\text{RIP}} = I_{\text{DD}} / (F_{\text{CLK}} \times C_F)
\]

\[
= V_{\text{DD}} / (R_{\text{LOAD}} \times F_{\text{CLK}} \times C_F)
\]

\[
= 3.43 / (500K \times 50 \times 10\text{uF}) = 11.4mV
\]

Capacitor Isolation Examples

<table>
<thead>
<tr>
<th>(V_{\text{IN}})</th>
<th>(V_{\text{DD}}) Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>(3.0V_{p-p})</td>
<td>2.20V 4mV</td>
</tr>
<tr>
<td>(3.0V_{p-p})</td>
<td>2.16V 4mV</td>
</tr>
<tr>
<td>(3.0V_{p-p})</td>
<td>2.07V 4mV</td>
</tr>
<tr>
<td>(5.0V_{p-p})</td>
<td>3.50V 7mV</td>
</tr>
<tr>
<td>(5.0V_{p-p})</td>
<td>3.50V 15mV</td>
</tr>
<tr>
<td>(12V_{\text{RMS}})</td>
<td>3.20V 11mV</td>
</tr>
<tr>
<td>(24V_{\text{RMS}})</td>
<td>3.43V 11mV</td>
</tr>
</tbody>
</table>

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