



CSS NVM

NV Register Application Note #1 – Margin Test Mode

CSS Nonvolatile Memory Library

Margin Test Mode

A special test mode has been included to provide a means to insure the integrity of the nonvolatile data. The Margin test is intended to be used as part of a production screen, to provide added assurance that the EE cells are programming adequately. If performed as a “Go – No Go” test using a single Margin current level, it can be performed very quickly and adds very little to the total test time.

Each bit of nonvolatile memory contains a differential memory circuit. One EE cell is programmed to an “OFF” state, the other is programmed “ON”. During the Margin test mode, a test current, “ I_M ”, is applied to the “ON” cell. If the cell fails to maintain its current logic state while sinking the test current, a weak bit is indicated. The test result of each bit is logically OR’ed. If any EE cell fails, the “MFAIL” signal goes to a logic one, indicating a failure.

The Margin test mode is entered by taking the MRG_EN input high while in Read mode. The Margin mode enables the VMRGN input, an analog voltage within a current mirror (but driven by an external test current). (Please refer to Table #1, Block Diagram #1 and the Timing Diagrams.) To check the programming margin of the EE cells, a small current, “ I_M ”, is sunk from the I_MRGN pin to VSS. Increasing I_M makes it more difficult for an “ON” EE cell to hold its logic state. Typical values for I_M are 5 μ A to 10 μ A.

A typical “Go – No Go” Margin test sequence might be:

- 1) Erase all bits to “0”
- 2) Read all bits without Margin (verify normal Read)
- 3) Enable the Margin mode, enable I_M sink (~5 μ A) and check MFAIL signal
- 4) Write all bits to “1”
- 5) Read all bits without Margin (verify normal Read)
- 6) Enable the Margin mode, enable I_M sink (~5 μ A) and check MFAIL signal

To characterize the pass/fail point for each bit, repeat steps #1 through #6, while increasing I_M . (Wait at least 10 μ s between changing I_M and checking the MFAIL signal to allow the Bias Current Generator to settle.)

Note – A full functional test for the EEPROM should also include checkerboard and random patterns to identify near neighbor and decoder defects.

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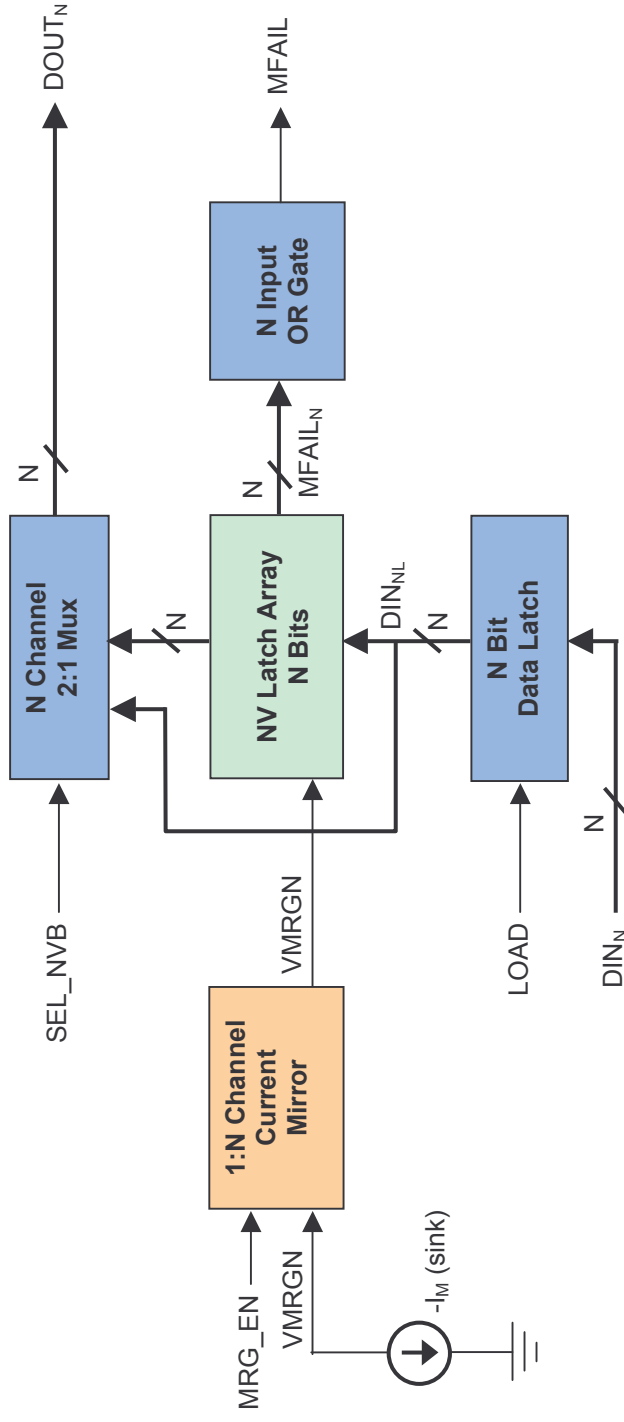
Read Modes

Mode	Description	PROGB	LOAD	SEL_NV B	MRG_EN	VMRGN	MFAIL	DIN _N	DOUT _N
Read	Read Mode (low current)	1	0	0	0	Open	0	X	NV Out _N
Margin Read	Read with Margin	1	0	0	1	Open	1 = Fail	X	NV Out _N
Load DIN	Load DIN Register	1	1	0	0	+I _M (sink)	0	Valid	NV Out _N
Select DIN	DOUT = DIN Register	1	0	1	0	VDD	0	X	DIN _{NL}

Table 1

Note: DIN_{NL} = Latched DIN_N

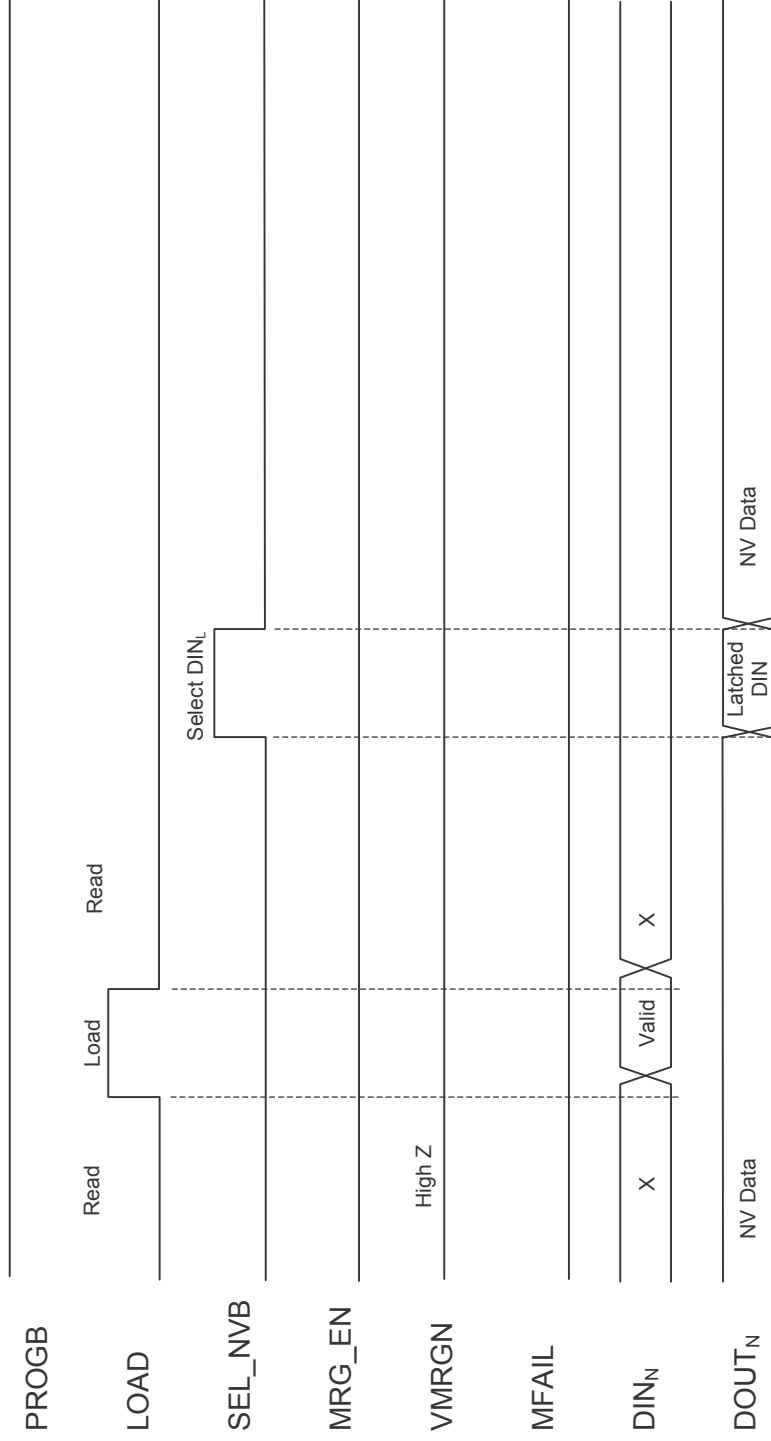
Margin Mode Block Diagram



Block Diagram 1

Timing Diagrams

Read, Load DIN and Select Latched DIN



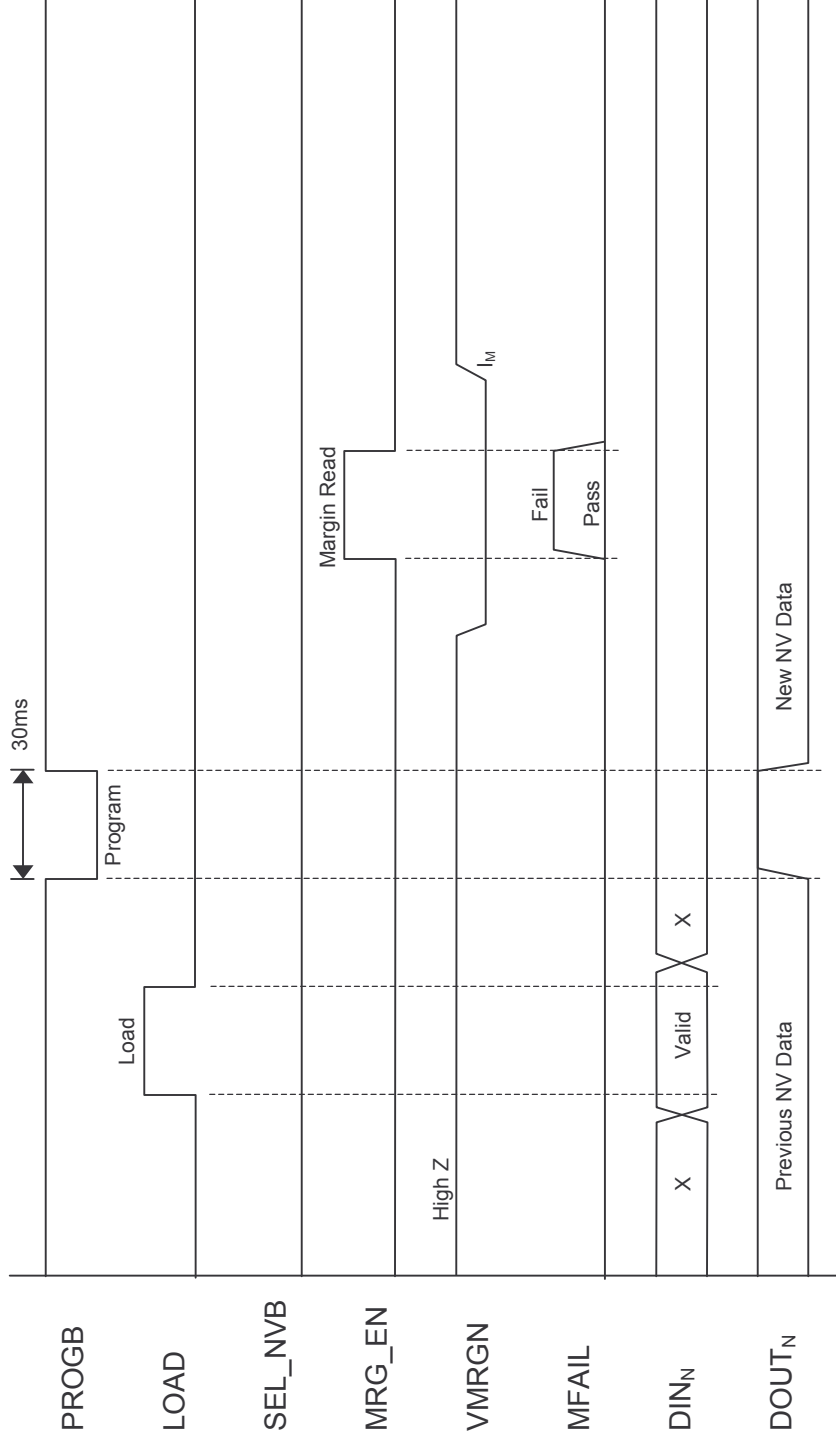
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Timing Diagrams

Load DIN, Program NV Memory and Read with Margin



Timing Diagrams

Load DIN, Program NV Memory (Data always valid) and Read with Margin

