CSS MEM

Low Power SRAM Macro (C5 Process)

CSS Memory Library

General Description

The SRAM memory macro cell is an ultra low power, Static Random Access Memory. The Read and Write mode circuits have been designed for a wide supply range and very low power. The memory architecture can be configured in a variety of sizes, from less than 1K bits up to 16K bits. The number of bits per byte may range from 1 to 64. The bit line multiplexer may be configured 2:1, 4:1 or 8:1, allowing the aspect ratio of the physical layout to be optimized for the overall chip floor plan.

A low power standby mode has been included. The Read mode is synchronous. (Output data is valid after the rising edge of CE.) The output of the sense amplifier(s) is latched and held valid until the next read cycle. Data output signals have tri-state output drivers to facilitate a buss style architecture.

Features

- Ultra Low Power and Wide Supply Range
- Small Physical Size (Very compact memory core & periphery layout)
- Memory Architecture:
  - Memory Size = < 1K to >16K bits
  - Byte Size = 1 to 64 bits
  - Bit Line/Column Multiplexer Ratio = 2:1, 4:1 & 8:1
- Operating Modes:
  - Standby Mode (IDD ~ 0uA)
  - Read Mode = Synchronous
  - Write Mode
- Output Driver:
  - Tri-State for buss architectures
- Compatible with all C5 processes
  - Does NOT require Double Poly or Metal3

CSS Memory Library

Specification Summary

Process: any AMI C5 (double Poly, 1K Poly is NOT required)

Temperature range = -40ºC to +85ºC (military range available on request)

Supply Voltage:

1.25V to 5.5V

Supply Current:

Standby current = <100nA (junction leakage only)

Read current depends on memory size, architecture, cycle time and supply voltage (see tables for typical values)

Memory Size (Typical examples):

8K (1K x 8) = Physical size ~ 300µm x 390µm

32K (4K x 8) = Physical size ~ 480µm x 650µm

128K (16K x 8) = Physical size ~ 830µm x 1220µm

see Tables 2A and 2B for more examples

see "CSS_SRAM_C5X.xls" to calculate sizes for non-binary configurations

Read Access Time:

Access time depends on memory size, architecture and supply voltage (see tables for typical values)

Address & Data I/O

Address = ADDR[N:0]

Data Out = DOUT[N:0], tri-state (separate output enable (OE) signal)

Pin Descriptions

Power Pins

VDD Positive supply voltage.
VSS Ground.

Control Pins

CE Chip Enable. Read/Write cycles are initiated on each rising edge.
RD Read. Enables Read mode. (active high)
WR Write. Enables Write mode. (active high)
OE Output enable. Enables Data Out output driver. (Logic low = High Z.)

Address Pins

ADDR[N:0] Row and column address lines. Used to select 1 of $(N+1)^2$ address locations.

Data I/O Pins

DIN[N:0] N Data input lines.
DOUT[N:0] N Data output lines. (These are tri-state outputs.)

Operating Modes

Standby Standby/Low current mode
Read Accesses one word of data from the memory array.
Write Writes one word of data into the memory array.

A summary of the operating modes is provided in Table 1.

Read Modes

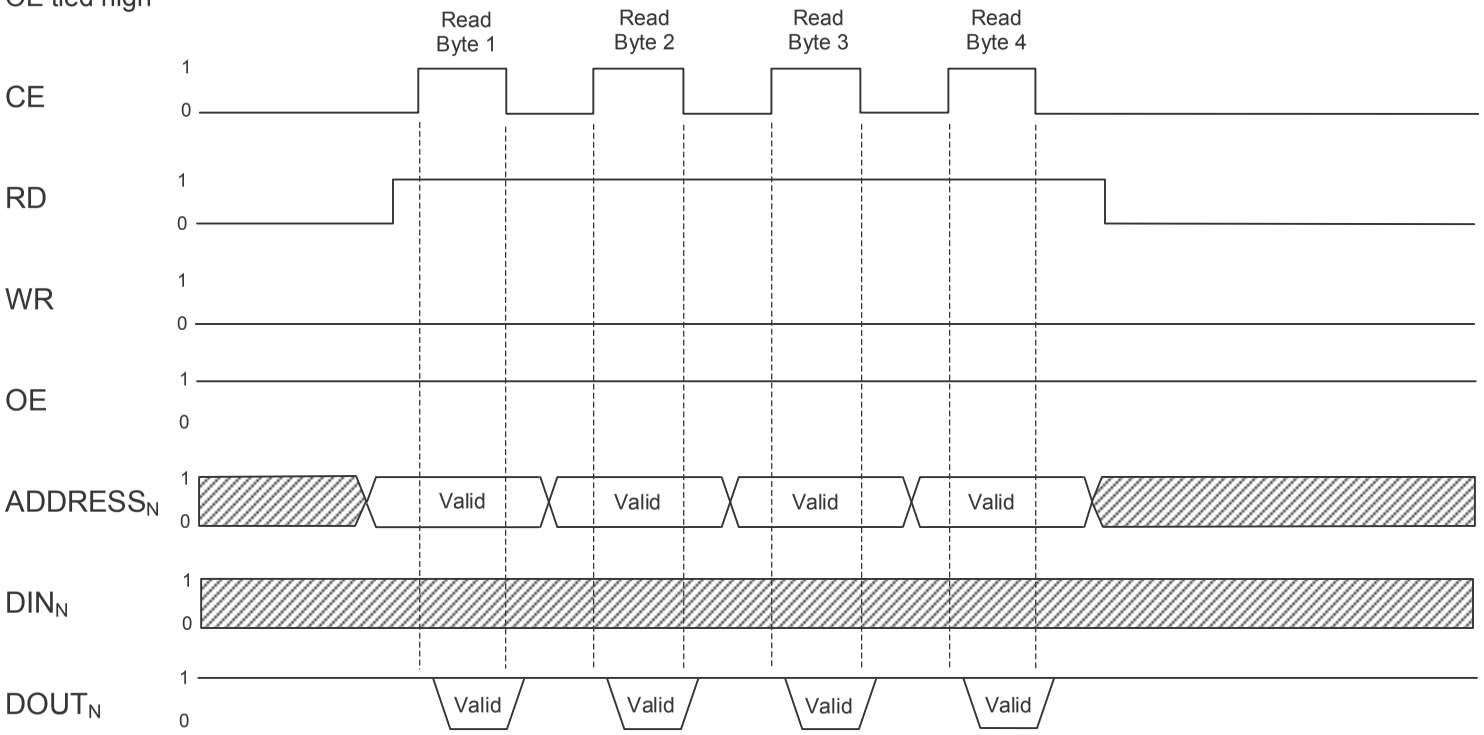
Mode	Description	CE	RD	WR	OE	$ADDR_N$	DIN_N	$DOUT_N$
Standby	Low Current Standby	0	0	0	0 1	X	X	High Z 1
Read	Read Data	1	1	0	1	Valid	X	$DOUT_N$
Write	Write Data	1	0	1	0	Valid	Valid	High Z

Table 1

Timing Diagrams

Read 4 Bytes

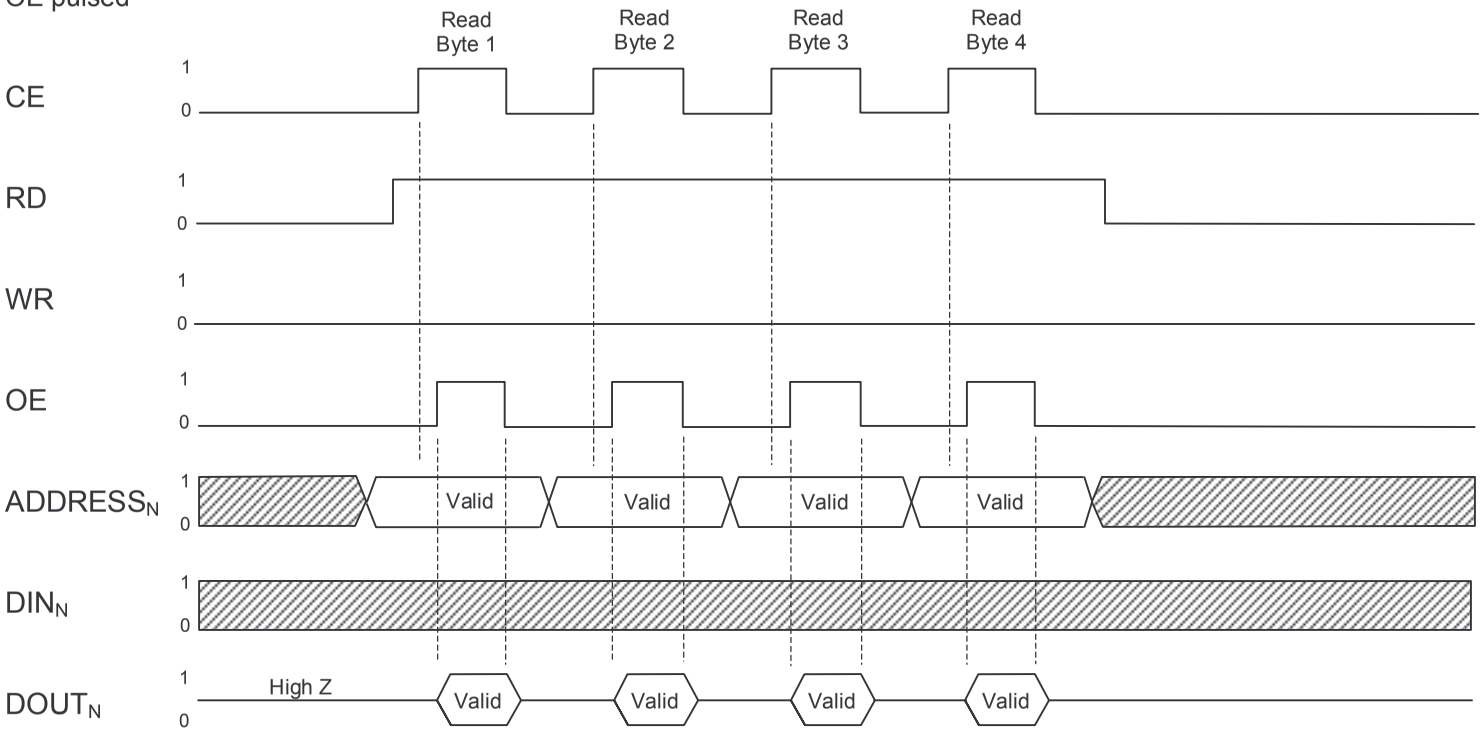
OE tied high



Timing Diagrams

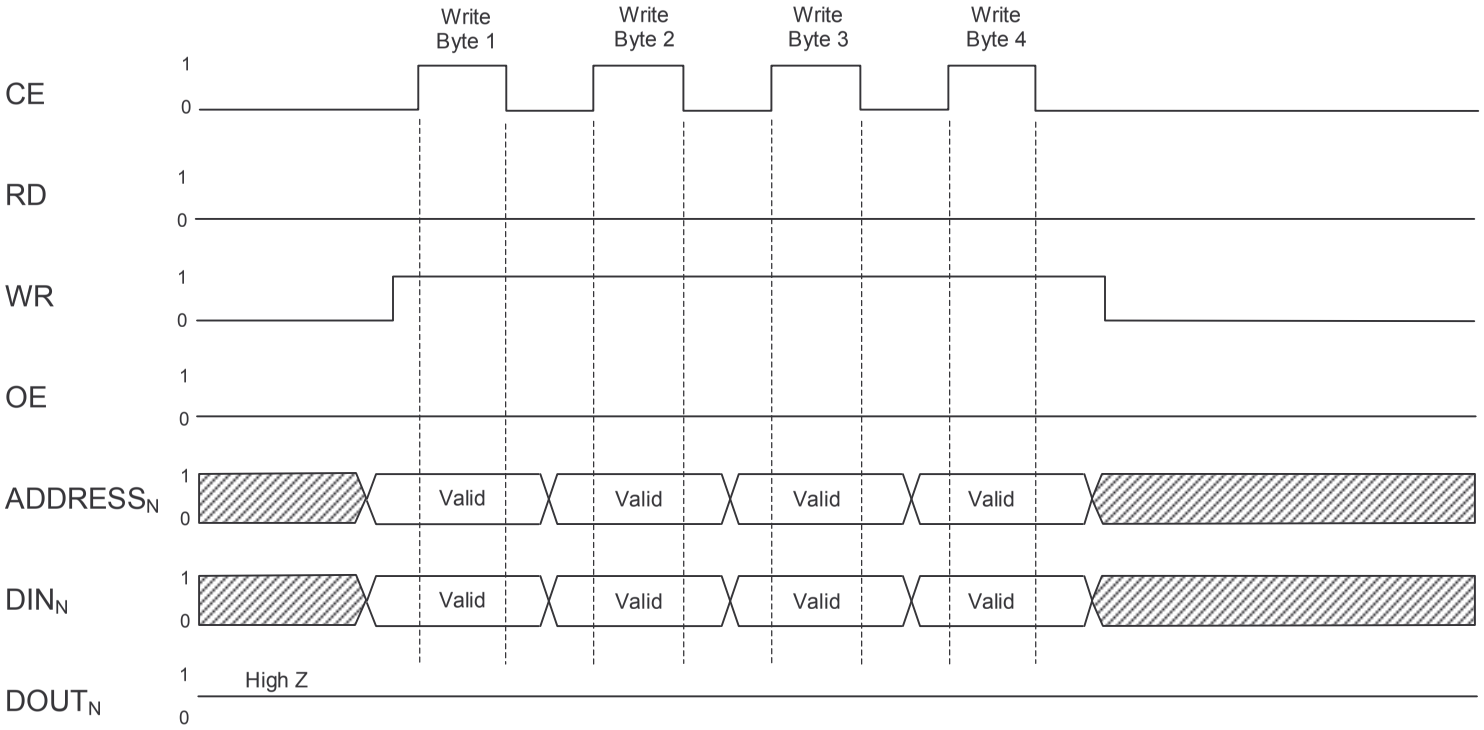
Read 4 Bytes

OE pulsed

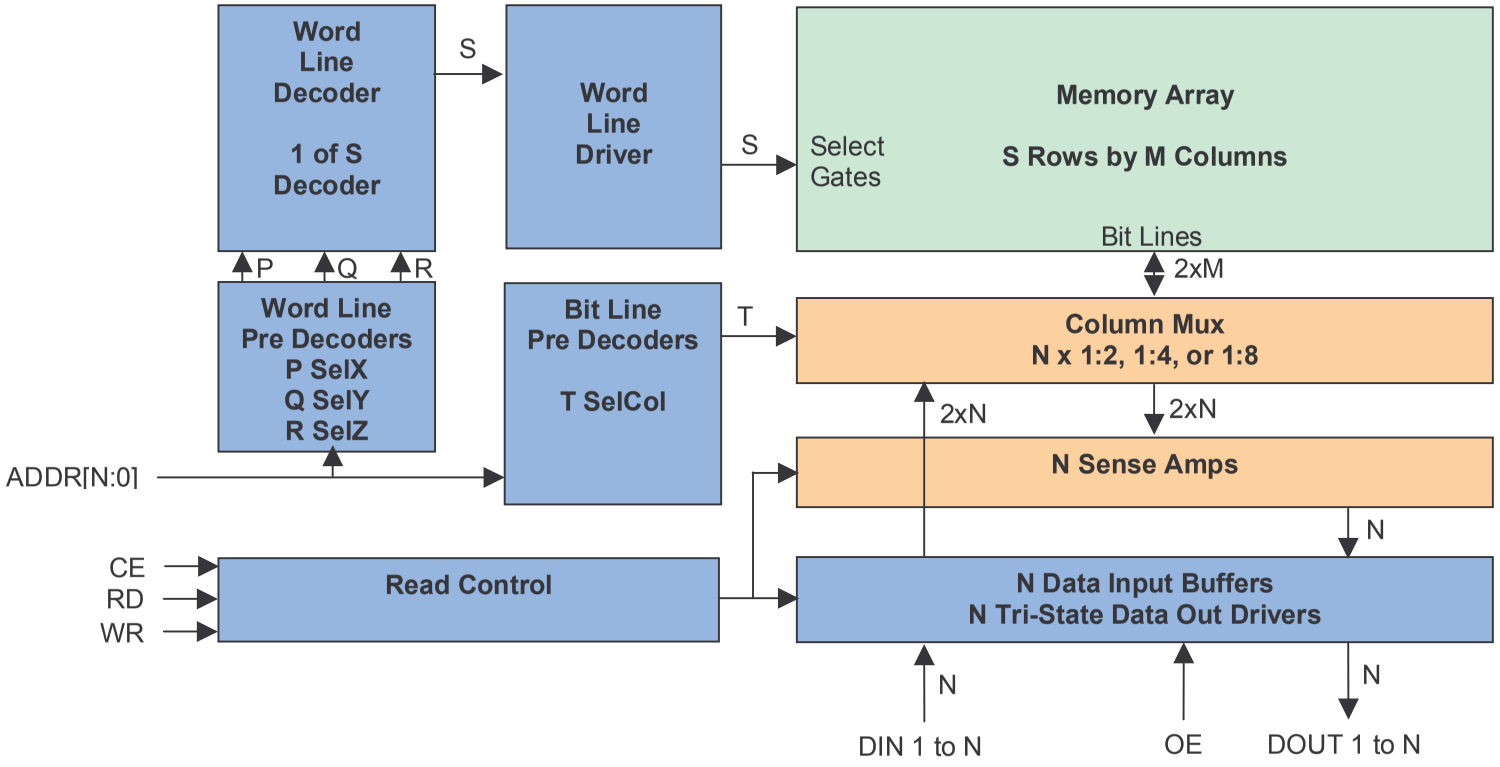


Timing Diagrams

Write 4 Bytes



SRAM Block Diagram



C5 SRAM Area for Typical Memory Configurations

	SRAM Area (square microns) vs. Number of Bytes								
Bits/Byte	8	16	32	64	128	256	512	1K	2K
1	11520	12360	15670	20100	29320	49960	91480	185810	419710
2	13600	16140	20580	29380	42480	70890	127960	253380	549450
4	17760	22220	30080	43200	68810	112770	200910	388520	808940
8	26070	32470	45630	69970	113960	196510	346830	658790	1327930
16	42690	52980	73910	118030	198590	348940	638670	1199340	2365890
32	75930	93990	130470	205670	356120	642550	1203270	2280430	4441820
64	142420	176020	243590	380970	655770	1216670	2287910	4442610	8593670

Table 2A

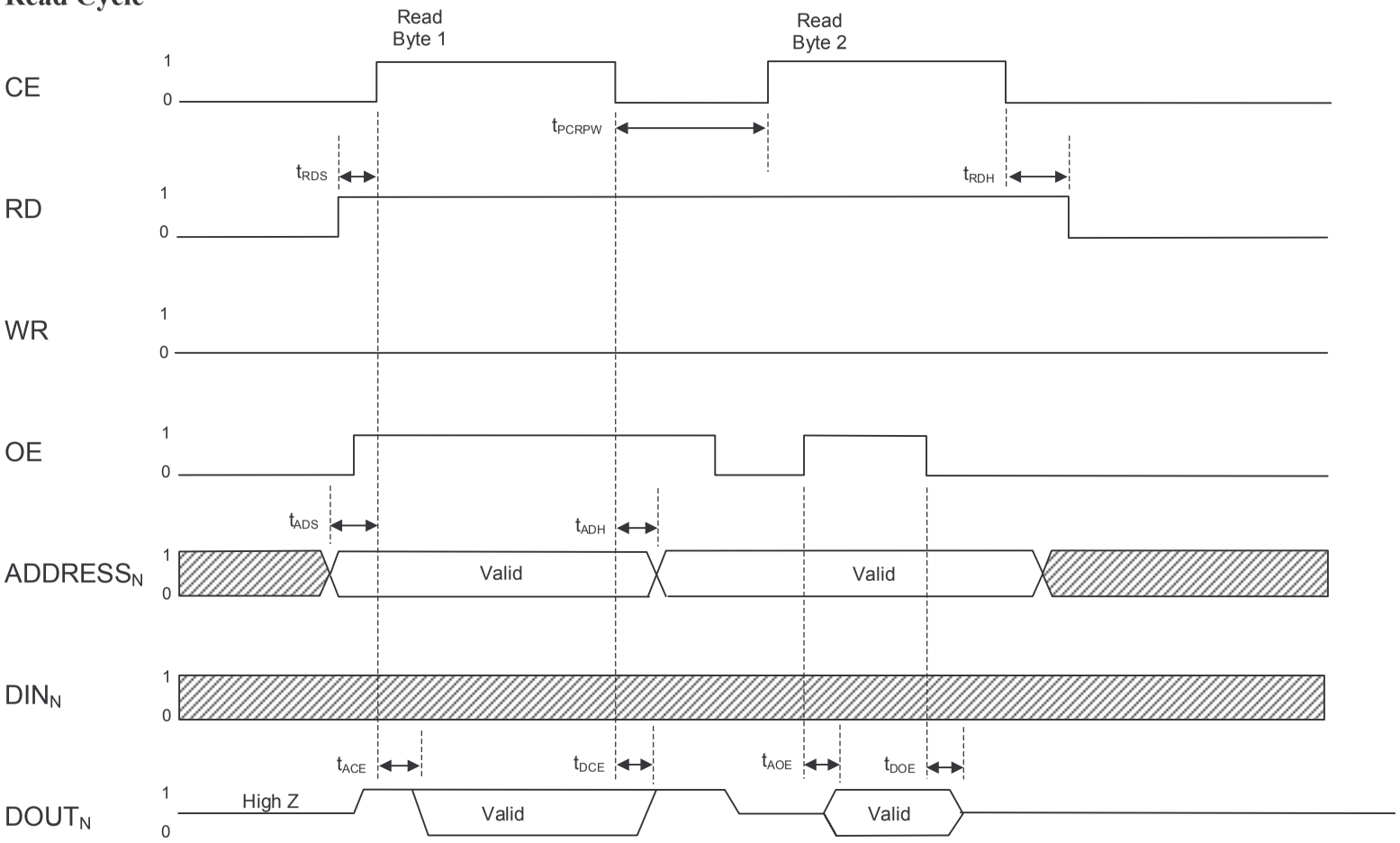
	SRAM Area (square mils) vs. Number of Bytes								
Bits/Byte	8	16	32	64	128	256	512	1K	2K
1	17.9	19.2	24.3	31.2	45.4	77.4	141.8	288.0	650.5
2	21.1	25.0	31.9	45.5	65.8	109.9	198.3	392.7	851.7
4	27.5	34.4	46.4	67.0	106.7	174.8	311.4	602.2	1253.9
8	40.4	50.3	70.7	108.4	176.6	304.6	537.6	1021.1	2058.3
16	66.2	82.1	114.6	182.9	307.8	540.9	989.9	1859.0	3667.1
32	117.7	145.7	202.2	318.8	552.0	996.0	1865.1	3534.7	6884.8
64	220.7	272.8	377.6	590.5	1016.4	1885.8	3546.3	6886.1	13320.2

Table 2B

Use the SRAM Calculator ("CSS_SRAM_C5X.xls") to determine actual X, Y dimensions, including non-binary configurations.

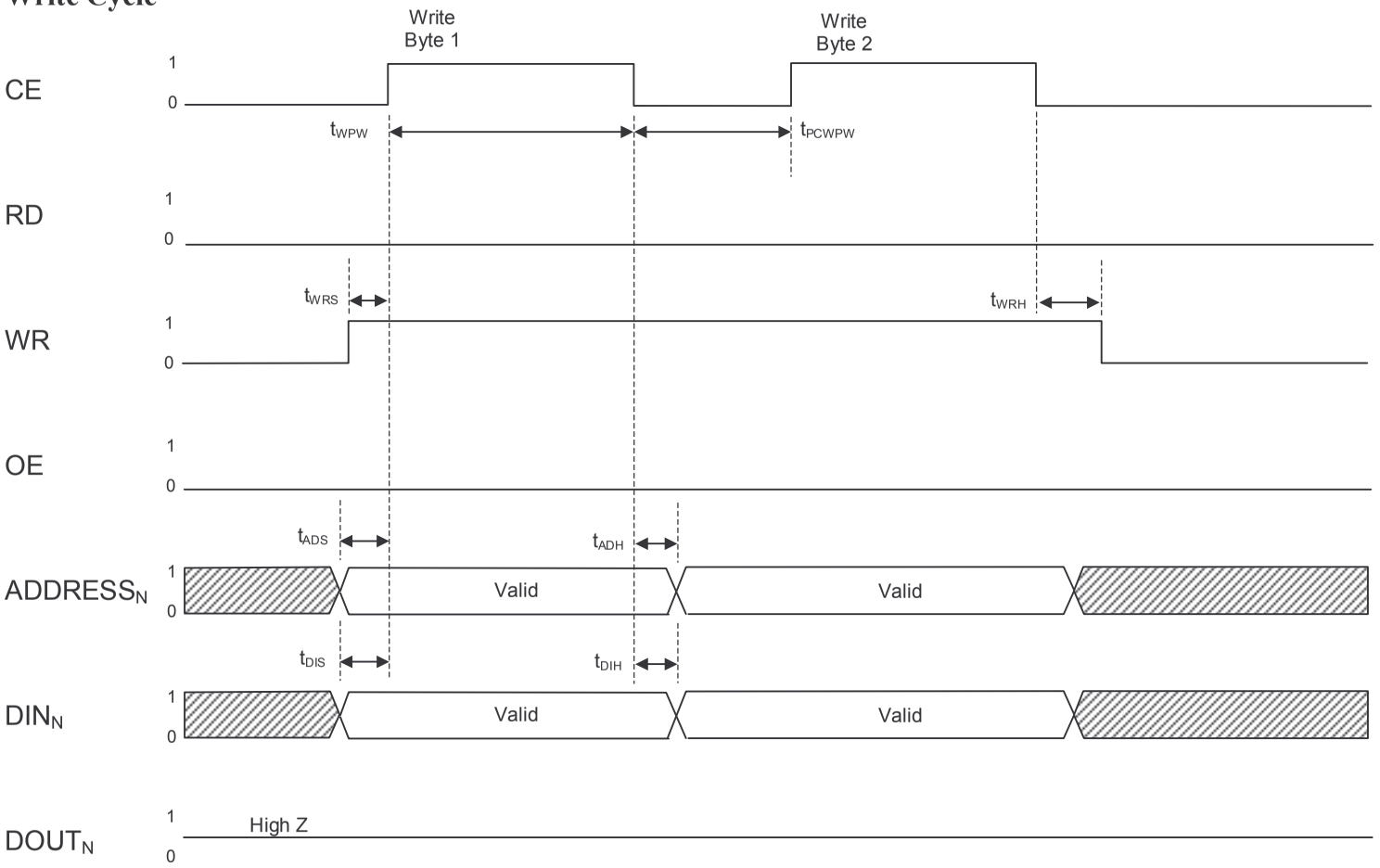
Timing Specifications

Read Cycle



Timing Specifications

Write Cycle



AC/DC Electrical Specifications (from SPICE)

Operating Conditions:

VDD = 1.5V ±40mV%

Temperature = +18ºC to +40ºC

Read Cycle

Parameter	Symbol	Conditions	Min.	Typical	Max.	Units
VDD Static Current	I_{DD0}	CE, RD, WR = 0		< 0.1	< 0.1	uA
VDD Active Read Current	I_{DDR}	CE, RD = 1 MHz, WR = 0, OE = 1	32	36	40	uA
Pre-charge Pulse Width (Read)	t_{PCRPW}	CE low to CE high	6.6	11	18	nsec
RD Setup Time	t_{RDS}	RD high to CE high	0	0	0	nsec
RD Hold Time	t_{RDH}	CE low to RD low	0	0	0	nsec
Address Setup Time	t_{ADS}	Address valid to CE high	-3.2	-5.5	-9.4	nsec
Address Hold Time	t_{ADH}	CE low to address change	3.7	5.9	10	nsec
Read Access time from CE	t_{ACE}	CE high to DOUT valid	30	54	99	nsec
Read Access time from OE	t_{AOE}	OE high to DOUT valid	5.0	7.9	14	nsec
Data Out Invalid Delay	t_{DCE}	CE low to DOUT invalid	9.3	15	26	nsec
Data Out Disable Delay	t_{DOE}	OE low to DOUT = High Z	1.1	1.6	3.0	nsec

Table 3A

Write Cycle

Parameter	Symbol	Conditions	Min.	Typical	Max.	Units
VDD Active Write Current	I_{DDW}	CE, WR = 1 MHz, RD = 0, OE = 0	25	29	32	uA
Pre-charge Pulse Width (Write)	t_{PCWPW}	CE low to CE high	6.6	11	18	nsec
Write Pulse Width	t_{WPW}	CE high to CE low	13	21	38	nsec
WR Setup Time	t_{WRS}	WR high to CE high	0	0	0	nsec
WR Hold Time	t_{WRH}	CE low to WR low	0	0	0	nsec
Address Setup Time	t_{ADS}	Address valid to CE high	-3.2	-5.5	-9.4	nsec
Address Hold Time	t_{ADH}	CE low to address change	3.7	5.9	10	nsec
Data In Setup Time	t_{DIS}	DIN valid to CE high	-7.1	-12	-20	nsec
Data In Hold Time	t_{DIH}	CE low to DIN change	2.7	4.4	7.2	nsec

Table 3B

Notes:

DOUT C_{LOAD} = 0.05 pF + 2 logic gate inputs

Delay times are measured from 50% to 50% levels

Port Input Load & Output Drive Summary

Ports

Port Name	Type	Description	Input Load	Output Drive High	Output Drive Low
CE	CMOS Input	Circuit Enable, Active High	2	N.A.	N.A.
RD	CMOS Input	Read, Active High	2	N.A.	N.A.
WR	CMOS Input	Write, Active High	2	N.A.	N.A.
OE	CMOS Input	Output Enable, Active High	2	N.A.	N.A.
$ADDR_N$	CMOS Input	Column Address Input (N)	2	N.A.	N.A.
$ADDR_N$	CMOS Input	Row Address Inputs (N)	1	N.A.	N.A.
DIN_N	CMOS Input	Data Inputs (N)	3	N.A.	N.A.
$DOUT_N$	Tri-State Output	Data Outputs (N)	N.A.	W/L = 3.0/0.6	W/L = 1.2/0.6

Table 4

Notes:
Input load is specified as the number of logic gate inputs. One input is: Pch W/L = 6.5/0.6, Nch W/L = 2.5/0.6
Output drive is listed as the W/L of the tri-state output gate. There are two series devices in the pull-up & pull-down paths.