



CSS MEM

Low Power SRAM Macro (C3 Process)

CSS Memory Library

General Description

The SRAM memory macro cell is an ultra low power, Static Random Access Memory. The Read and Write mode circuits have been designed for a wide supply range and very low power. The memory architecture can be configured in a variety of sizes, from less than 1K bits up to 16K bits. The number of bits per byte may range from 1 to 64. The bit line multiplexer may be configured 2:1, 4:1 or 8:1, allowing the aspect ratio of the physical layout to be optimized for the overall chip floor plan.

A low power standby mode has been included. The Read mode is synchronous. (Output data is valid after the rising edge of CE.) The output of the sense amplifier(s) is latched and held valid until the next read cycle. Data output signals have tri-state output drivers to facilitate a buss style architecture.

Features

- Ultra Low Power and Wide Supply Range
- Small Physical Size (Very compact memory core & periphery layout)
- Memory Architecture:
 - Memory Size = < 1K to > 16K bits
 - Byte Size = 1 to 64 bits
 - Bit Line/Column Multiplexer Ratio = 2:1, 4:1 & 8:1
- Operating Modes:
 - Standby Mode (IDD ~ 0uA)
 - Read Mode = Synchronous
 - Write Mode
- Output Driver:
 - Tri-State for buss architectures
- Compatible with all C3 processes
 - Does NOT require Double Poly or Metal3

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Specification Summary

Process: any AMI C3 (double Poly, 1K Poly is NOT required)

Temperature range = -40°C to +85°C (military range available on request)

Supply Voltage:
1.25V to 5.5V

Supply Current:

Standby current = <100nA (junction leakage only)

Read current depends on memory size, architecture, cycle time and supply voltage (see tables for typical values)

Memory Size (Typical examples):

8K (1K x 8) = Physical size ~ 300µm x 390µm

32K (4K x 8) = Physical size ~ 480µm x 650µm

128K (16K x 8) = Physical size ~ 830µm x 1220µm

see Tables 2A and 2B for more examples

see “CSS_SRAM_C3X.xls” to calculate sizes for non-binary configurations

Read Access Time:

Access time depends on memory size, architecture and supply voltage (see tables for typical values)

Address & Data I/O

Address = ADDR[N:0]

Data Out = DOUT[N:0], tri-state (separate output enable (OE) signal)

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Pin Descriptions

Power Pins

VDD Positive supply voltage.
VSS Ground.

Control Pins

CE Chip Enable. A Read cycle is initiated on each rising edge.
OE Output enable. Enables Data Out output driver. (Logic low = High Z.)

Address Pins

ADDR[N:0] Row and column address lines. Used to select 1 of $(N+1)^2$ address locations.

Data Out Pins

DOUT[N:0] Data output lines. (These are tri-state outputs.)

Operating Modes

Standby Standby/Low current mode

Read Accesses one word of data from the memory array and latches it into the output data register.

A summary of the operating modes is provided in Table 1.

Read Modes

Mode	Description	CE	OE	ADDR _N	DOUT _N
Standby1	Low Current Standby, DOUT = High Z	0	0	X	High Z
Standby2	Low Current Standby, DOUT = Last Valid Data	0	1	X	DOUT _{N-1}
Read1	Normal Read Mode, DOUT = High Z	1	0	Valid	High Z
Read2	Normal Read Mode, DOUT = New Valid Data	1	1	Valid	DOUT _N

Table 1

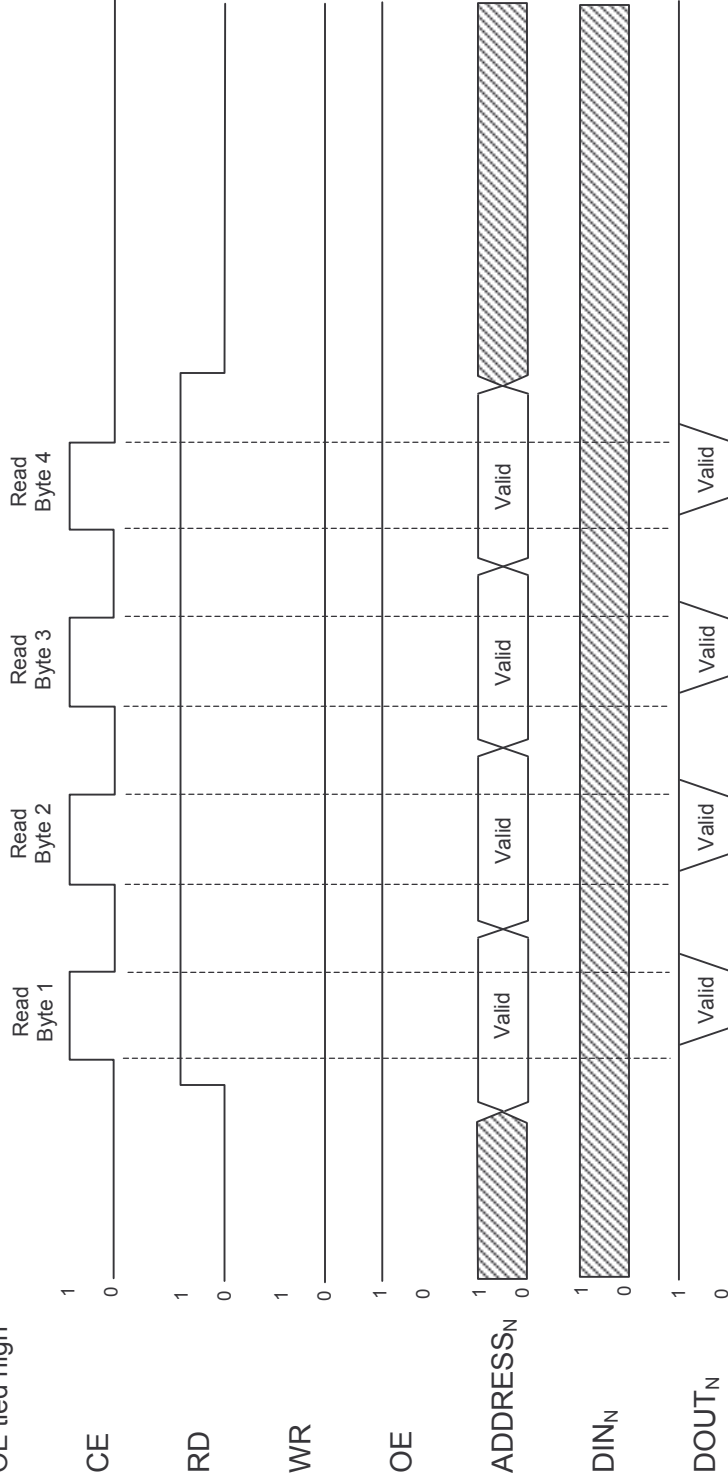
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Timing Diagrams

Read 4 Bytes
OE tied high



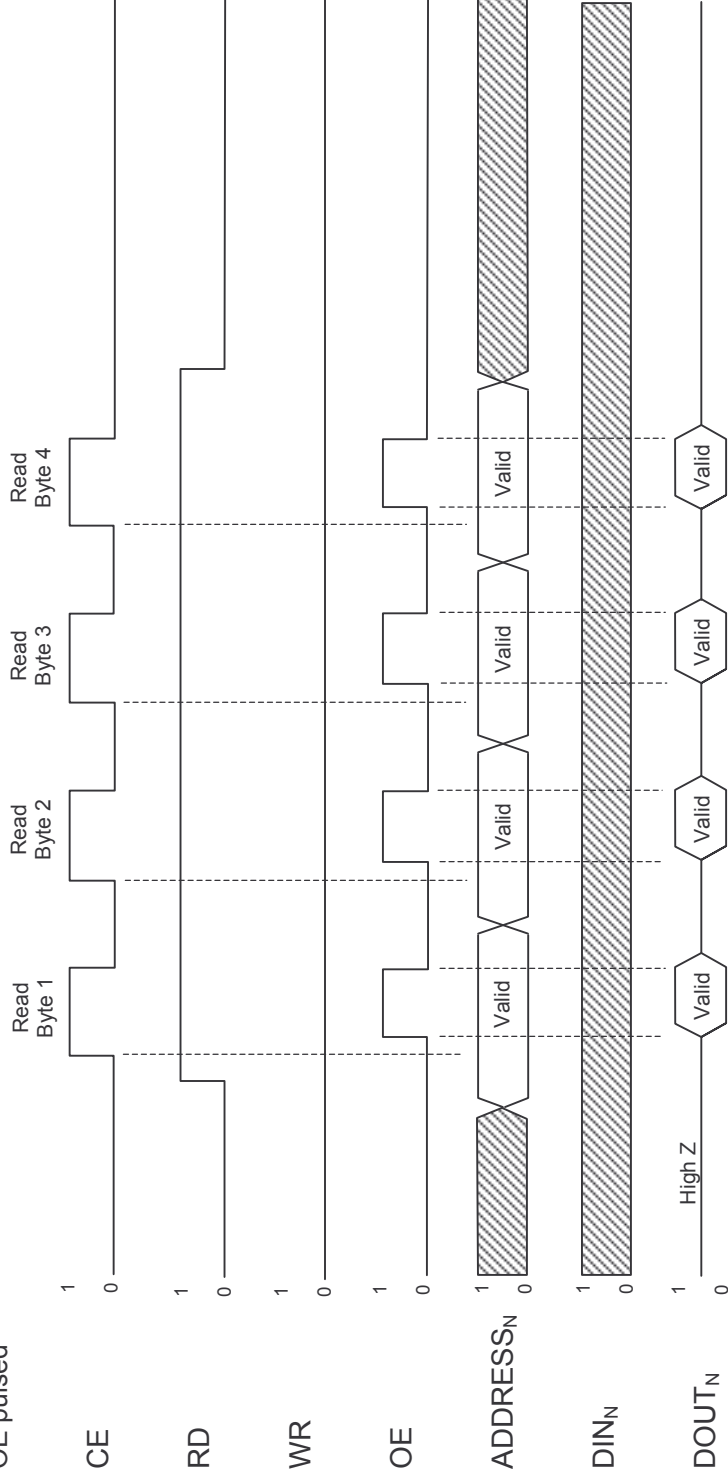
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Timing Diagrams

Read 4 Bytes
OE pulsed



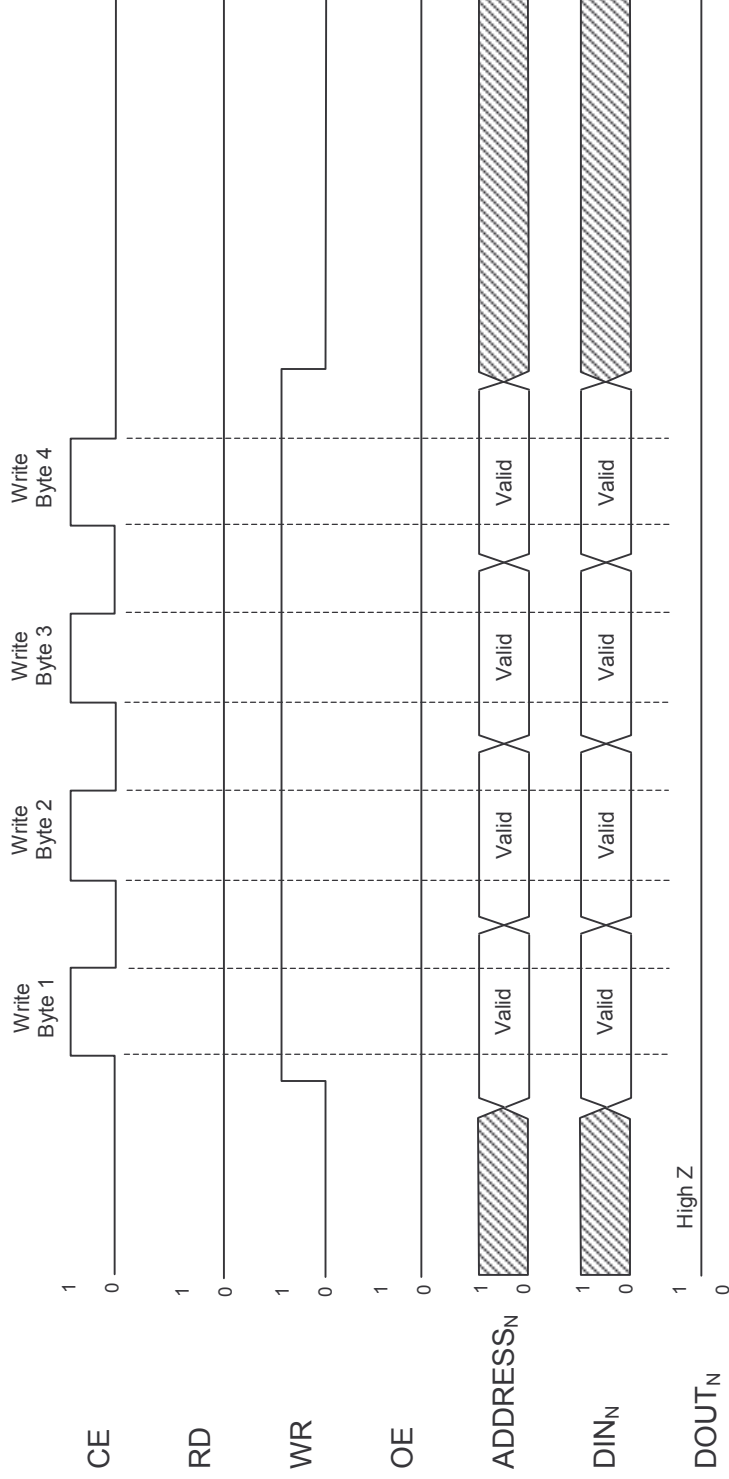
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Timing Diagrams

Write 4 Bytes

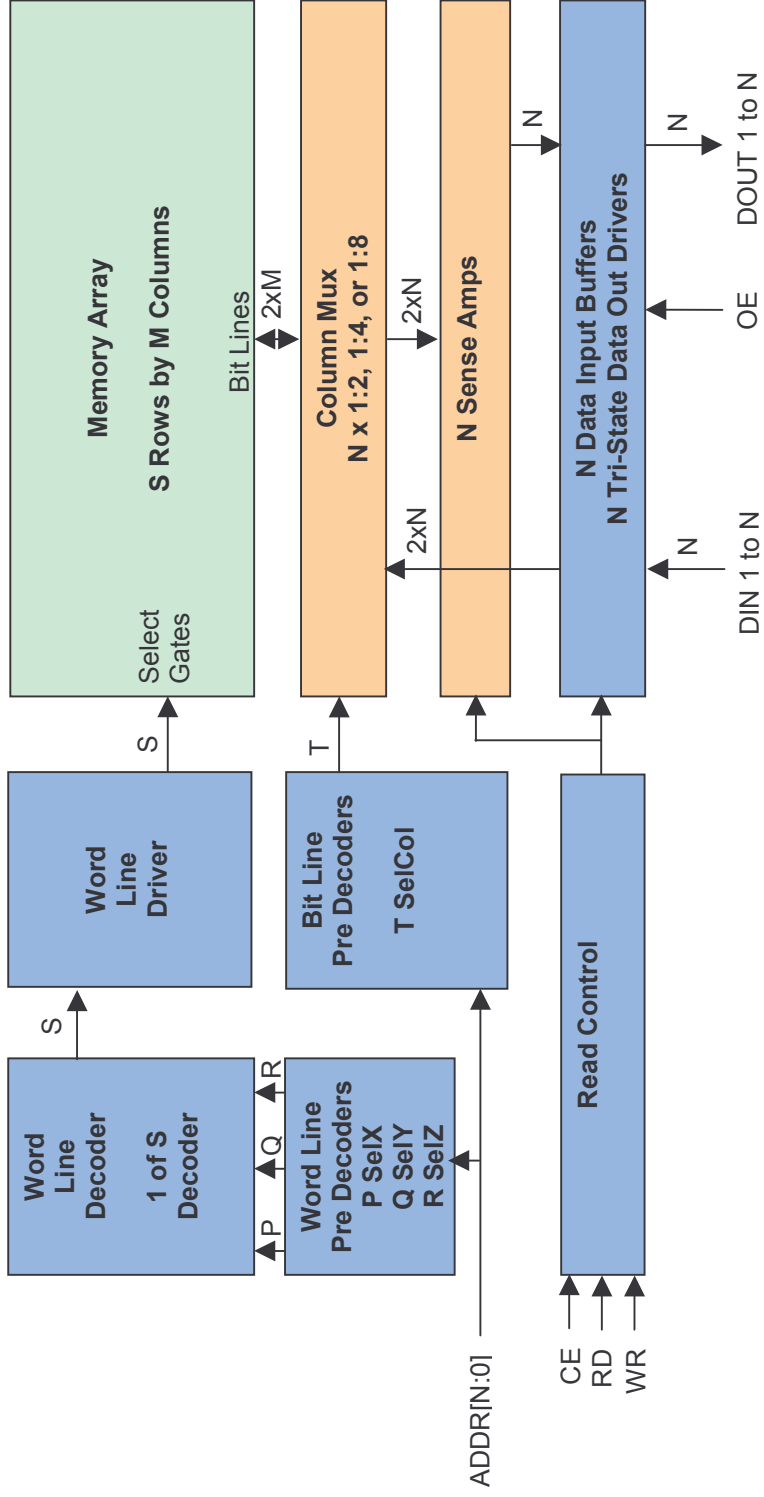


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C3 ROM Block Diagram



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C3 SRAM Area for Typical Memory Configurations

Bits/Byte	SRAM Area (square microns) vs. Number of Bytes									
	8	16	32	64	128	256	512	1K	2K	
1	5810	6350	8260	10800	15900	27510	50660	103080	232620	
2	6880	8330	10790	15860	23160	39160	71080	141080	305750	
4	9030	11490	15840	23150	37670	62460	111940	217080	452020	
8	13320	16880	24200	37650	62440	109050	193670	369070	744550	
16	21900	27660	39370	64210	109010	193630	357120	673060	1329600	
32	39060	49210	69710	112110	196770	357060	672990	1281040	2499710	
64	73380	92310	130380	207920	362840	678850	1280910	2496990	4839940	

Table 2A

Bits/Byte	SRAM Area (square mils) vs. Number of Bytes									
	8	16	32	64	128	256	512	1K	2K	
1	9.0	9.8	12.8	16.7	24.7	42.6	78.5	159.8	360.6	
2	10.7	12.9	16.7	24.6	35.9	60.7	110.2	218.7	473.9	
4	14.0	17.8	24.6	35.9	58.4	96.8	173.5	336.5	700.6	
8	20.6	26.2	37.5	58.4	96.8	169.0	300.2	572.1	1154.0	
16	33.9	42.9	61.0	99.5	169.0	300.1	553.5	1043.2	2060.9	
32	60.5	76.3	108.0	173.8	305.0	553.4	1043.1	1985.6	3874.6	
64	113.7	143.1	202.1	322.3	562.4	1052.2	1985.4	3870.3	7501.9	

Table 2B

Use the SRAM Calculator (“CSS_SRAM_C3X.xls”) to determine actual X, Y dimensions, including non-binary configurations.