



CSS NVM

Low Power ROM Macro (C5 Process)

CSS Nonvolatile Memory Library

General Description

The ROM memory macro cell is an ultra low power, Read Only Memory. The Read mode circuits have been designed for a wide supply range and very low power. The memory architecture can be configured in a variety of sizes, from less than 1K bits up to 256K bits. The number of bits per byte may range from 1 to 64. The bit line multiplexer may be configured 8:1, 16:1 or 32:1, allowing the aspect ratio of the physical layout to be optimized for the overall chip floor plan. Programming is accomplished via one mask layer (Active).

A low power standby mode has been included. The Read mode is synchronous. (Output data is valid after the rising edge of CE.) The output of the sense amplifier(s) is latched and held valid until the next read cycle. Data output signals have tri-state output drivers to facilitate a buss style architecture.

Features

- Ultra Low Power and Wide Supply Range
- Small Physical Size (Very compact memory core & periphery layout)
- Memory Architecture:
 - Memory Size = < 1K to >256K bits
 - Byte Size = 1 to 64 bits
 - Bit Line/Column Multiplexer Ratio = 8:1, 16:1 & 32:1
- Operating Modes:
 - Standby Mode (IDD ~ 0uA)
 - Read Mode = Synchronous
- Output Driver:
 - Tri-State for buss architectures
- Compatible with all C5 processes
 - Does NOT require Double Poly or Metal3

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Specification Summary

Process: any AMI C5 (double Poly, 1K Poly is NOT required)

Temperature range = -40°C to +85°C (military range available on request)

Supply Voltage:
1.25V to 5.5V

Supply Current:

Standby current = <100nA (junction leakage only)

Read current depends on memory size, architecture, cycle time and supply voltage (see tables for typical values)

Memory Size (Typical examples):

8K (1K x 8) = Physical size ~ 470µm x 225µm

32K (4K x 8) = Physical size ~ 820µm x 375µm

128K (16K x 8) = Physical size ~ 830µm x 1220µm

see Tables 2A and 2B for more examples

see “CSS_ROM_C5X.xls” to calculate sizes for non-binary configurations

Read Access Time:

Access time depends on memory size, architecture and supply voltage (see tables for typical values)

Address & Data I/O

Address = ADDR[N:0]

Data Out = DOUT[N:0], tri-state (separate output enable (OE) signal)

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Pin Descriptions

Power Pins

VDD Positive supply voltage.
VSS Ground.

Control Pins

CE Chip Enable. A Read cycle is initiated on each rising edge.
OE Output enable. Enables Data Out output driver. (Logic low = High Z.)

Address Pins

ADDR[N:0] Row and column address lines. Used to select 1 of $(N+1)^2$ address locations.

Data Out Pins

DOUT[N:0] Data output lines. (These are tri-state outputs.)

Operating Modes

Standby Standby/Low current mode

Read Accesses one word of data from the memory array and latches it into the output data register.

A summary of the operating modes is provided in Table 1.

Read Modes

Mode	Description	CE	OE	ADDR _N	DOUT _N
Standby1	Low Current Standby, DOUT = High Z	0	0	X	High Z
Standby2	Low Current Standby, DOUT = Last Valid Data	0	1	X	DOUT _{N-1}
Read1	Normal Read Mode, DOUT = High Z	1	0	Valid	High Z
Read2	Normal Read Mode, DOUT = New Valid Data	1	1	Valid	DOUT _N

Table 1

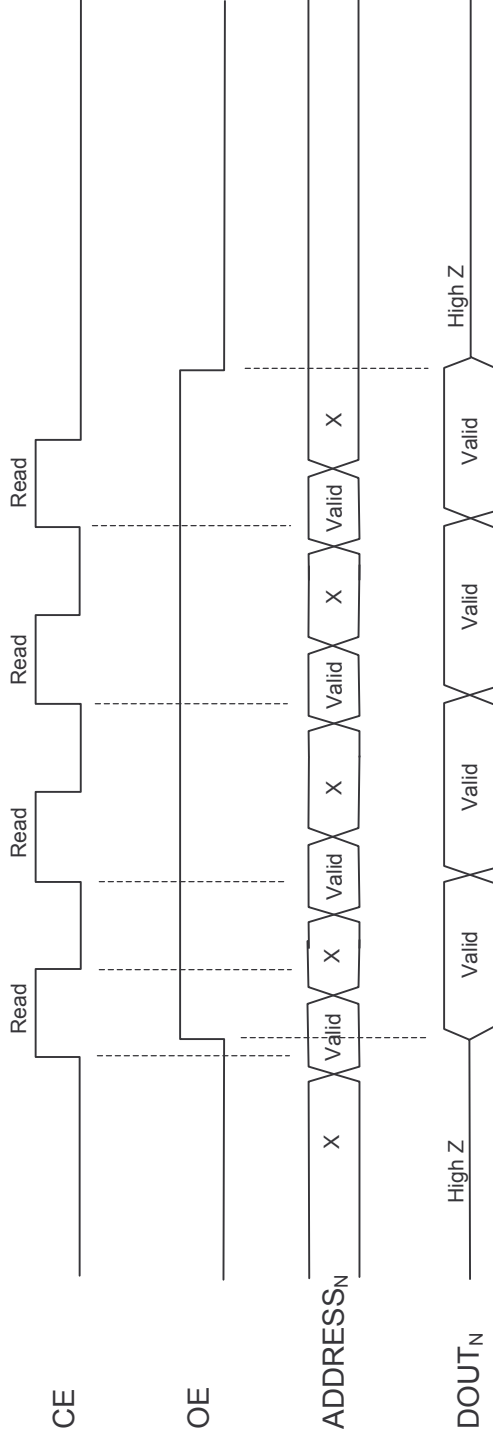
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Timing Diagrams

Read 4 Bytes

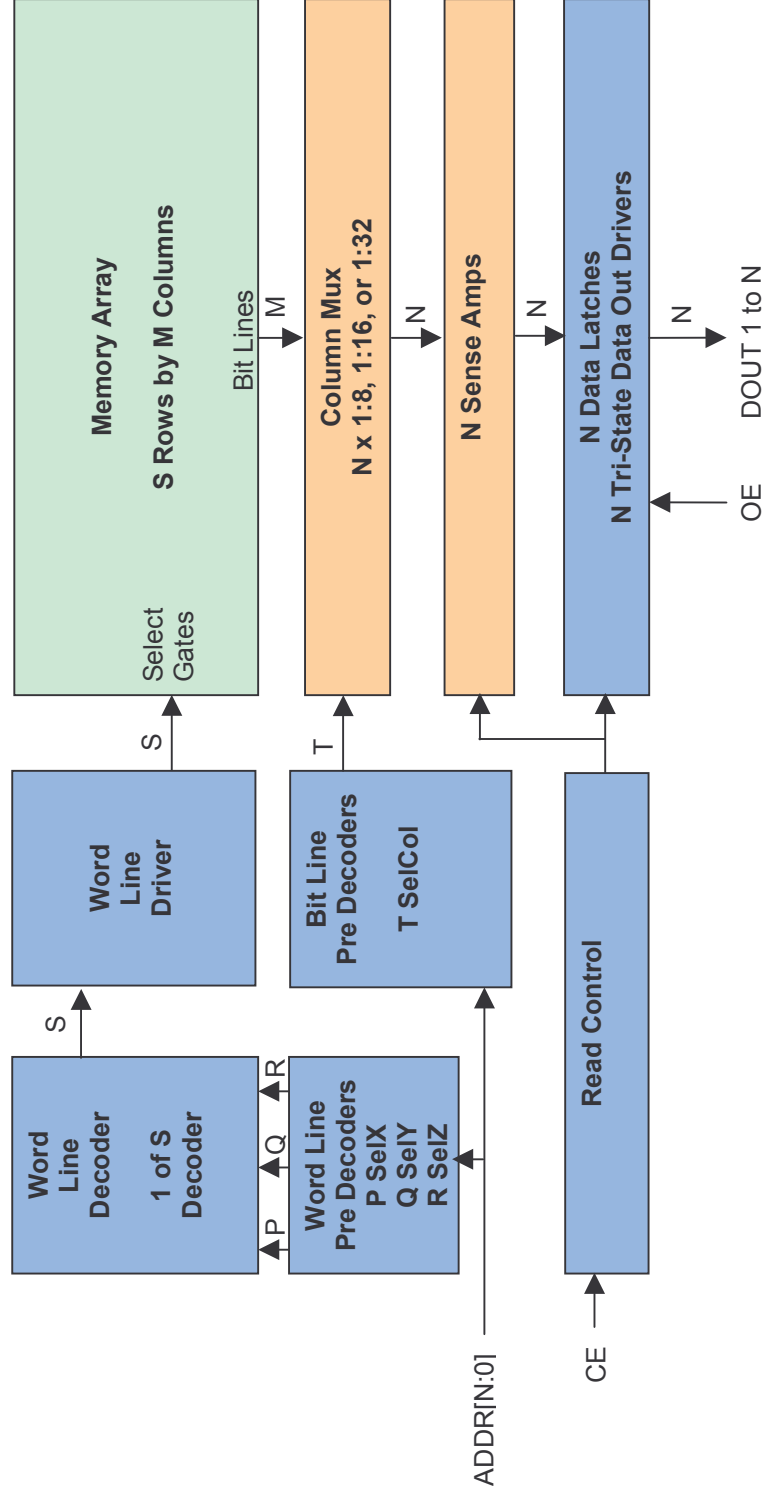


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C5 ROM Block Diagram



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C5 ROM Area for Typical Memory Configurations

Bits/Byte	ROM Area (square microns) vs. Number of Bytes									
	64	128	256	512	1K	2K	4K	8K	16K	
1	16810	16810	19710	26330	34550	49570	80140	142460	271840	
2	20300	21200	24850	33030	48060	69550	112230	198770	376580	
4	25600	29260	35140	46350	67430	109510	176400	311380	586050	
8	36200	41370	52690	72970	106160	173050	304750	536590	1005010	
16	57390	65590	82970	116150	183070	298950	530770	987030	1842930	
32	99770	114020	143510	200920	316270	548150	976320	1832180	3518760	
64	184530	210890	264600	370440	582660	1008280	1864260	3498240	6778820	

Table 2A

Bits/Byte	ROM Area (square mils) vs. Number of Bytes									
	64	128	256	512	1K	2K	4K	8K	16K	
1	26.1	26.1	30.6	40.8	53.6	76.8	124.2	220.8	421.3	
2	31.5	32.9	38.5	51.2	74.5	107.8	174.0	308.1	583.7	
4	39.7	45.4	54.5	71.8	104.5	169.7	273.4	482.6	908.4	
8	56.1	64.1	81.7	113.1	164.5	268.2	472.4	831.7	1557.8	
16	88.9	101.7	128.6	180.0	283.8	463.4	822.7	1529.9	2856.5	
32	154.6	176.7	222.4	311.4	490.2	849.6	1513.3	2839.9	5454.1	
64	286.0	326.9	410.1	574.2	903.1	1562.8	2889.6	5422.3	10507.2	

Table 2B

Use the ROM Calculator (“CSS_ROM_C5X.xls”) to determine actual X, Y dimensions, including non-binary configurations.