



## CSS NVM

## Low Power ROM Macro (C3 Process)

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### CSS Nonvolatile Memory Library

#### General Description

The ROM memory macro cell is an ultra low power, Read Only Memory. The Read mode circuits have been designed for a wide supply range and very low power. The memory architecture can be configured in a variety of sizes, from less than 1K bits up to 256K bits. The number of bits per byte may range from 1 to 64. The bit line multiplexer may be configured 8:1, 16:1 or 32:1, allowing the aspect ratio of the physical layout to be optimized for the overall chip floor plan. Programming is accomplished via one mask layer.

A low power standby mode has been included. The Read mode is synchronous. (Output data is valid after the rising edge of CE.) The output of the sense amplifier(s) is latched and held valid until the next read cycle. Data output signals have tri-state output drivers to facilitate a buss style architecture.

#### Features

- Ultra Low Power and Wide Supply Range
- Small Physical Size (Very compact memory core & periphery layout)
- Memory Architecture:
  - Memory Size = < 1K to >256K bits
  - Byte Size = 1 to 64 bits
  - Bit Line/Column Multiplexer Ratio = 8:1, 16:1 & 32:1
- Operating Modes:
  - Standby Mode (IDD ~ 0uA)
  - Read Mode = Synchronous
- Output Driver:
  - Tri-State for buss architectures
- Compatible with all C3 processes
  - Does NOT require Double Poly or Metal3

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#### Specification Summary

Process: any AMI C3 (double Poly, 1K Poly and Metal3 are NOT required)

Temperature range = -40°C to +85°C (military range available on request)

Supply Voltage:  
1.25V to 5.5V

#### Supply Current:

Standby current = <100nA (junction leakage only)

Read current depends on memory size, architecture, cycle time and supply voltage (see tables for typical values)

#### Memory Size (Typical examples):

8K (1K x 8) = Physical size ~ 315µm x 165µm

32K (4K x 8) = Physical size ~ 530µm x 275µm

128K (16K x 8) = Physical size ~ 540µm x 890µm

see Tables 2A and 2B for more examples

see “CSS\_ROM\_C3X.xls” to calculate sizes for non-binary configurations

#### Programming Layer:

Active

#### Read Access Time:

Access time depends on memory size, architecture and supply voltage (see tables for typical values)

#### Address & Data I/O

Address = ADDR[N:0]

Data Out = DOUT[N:0], tri-state (separate output enable (OE) signal)

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### Pin Descriptions

#### Power Pins

**VDD** Positive supply voltage.  
**VSS** Ground.

#### Control Pins

**CE** Chip Enable. A Read cycle is initiated on each rising edge.  
**OE** Output enable. Enables Data Out output driver. (Logic low = High Z.)

#### Address Pins

**ADDR[N:0]** Row and column address lines. Used to select 1 of  $(N+1)^2$  address locations.

#### Data Out Pins

**DOUT[N:0]** Data output lines. (These are tri-state outputs.)

### Operating Modes

**Standby** Standby/Low current mode

**Read** Accesses one word of data from the memory array and latches it into the output data register.

A summary of the operating modes is provided in Table 1.

### Read Modes

Mode	Description	CE	OE	ADDR <sub>N</sub>	DOUT <sub>N</sub>
Standby1	Low Current Standby, DOUT = High Z	0	0	X	High Z
Standby2	Low Current Standby, DOUT = Last Valid Data	0	1	X	DOUT <sub>N-1</sub>
Read1	Normal Read Mode, DOUT = High Z	1	0	Valid	High Z
Read2	Normal Read Mode, DOUT = New Valid Data	1	1	Valid	DOUT <sub>N</sub>

**Table 1**

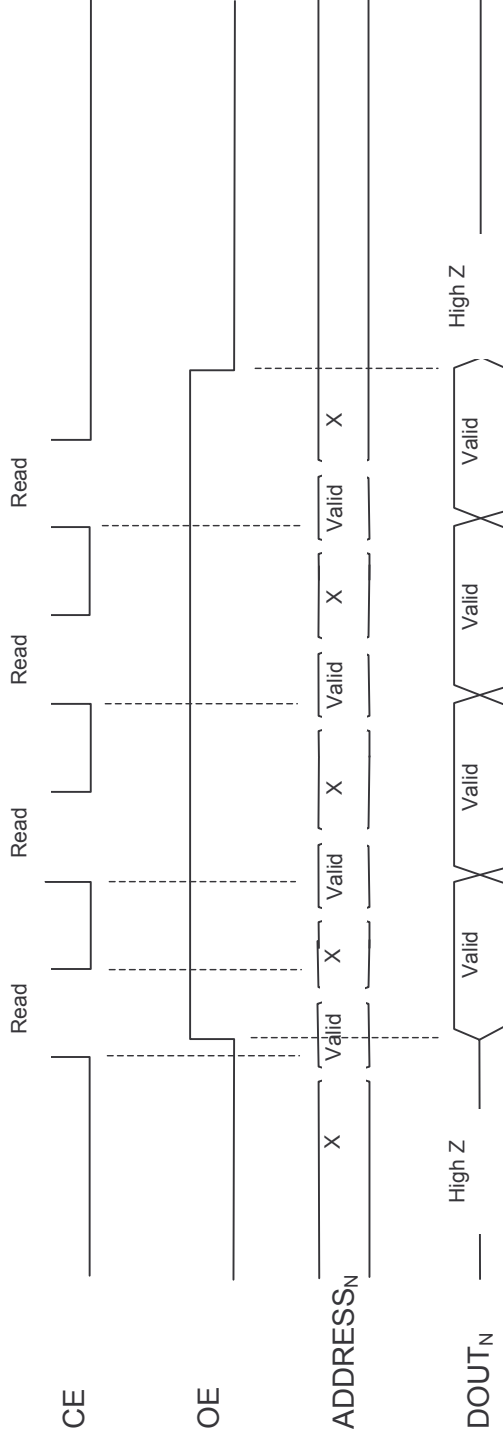
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### Timing Diagrams

Read 4 Bytes

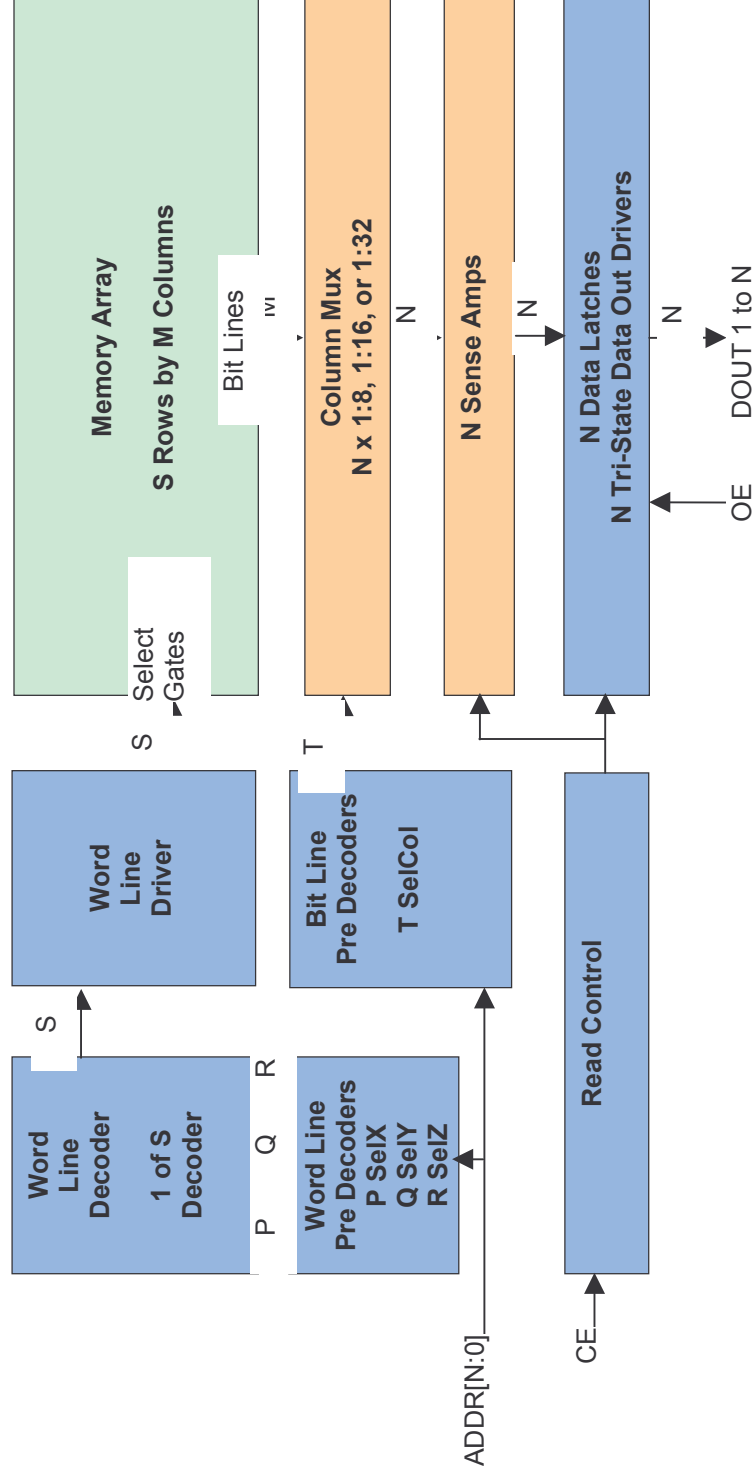


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## C3 ROM Block Diagram



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### C3 ROM Area for Typical Memory Configurations

Bits/Byte	ROM Area (square microns) vs. Number of Bytes									
	64	128	256	512	1K	2K	4K	8K	16K	
1	9100	9100	10620	13890	181500	25830	41500	73530	140370	
2	10780	11190	13060	17290	24720	35190	56440	99600	188630	
4	13260	15120	17930	23560	34030	53920	86300	151750	285340	
8	18210	20770	26460	36090	52130	84510	146030	256040	478760	
16	28110	32060	40540	56580	88340	143000	265500	464630	865610	
32	47910	54650	68700	95880	15560	259980	459110	860060	1639310	
64	87520	99820	125010	174480	273720	472870	871330	1628800	3154550	

Table 2A

Bits/Byte	ROM Area (square mils) vs. Number of Bytes									
	64	128	256	512	1K	2K	4K	8K	16K	
1	14.1	14.1	16.5	21.5	28.1	40.0	64.3	114.0	217.4	
2	16.7	17.3	20.2	26.8	38.3	54.6	87.5	154.4	292.4	
4	20.6	23.4	27.8	36.5	52.7	83.6	133.8	235.2	442.3	
8	28.2	32.2	41.0	55.9	80.8	131.0	226.4	396.9	742.1	
16	43.6	49.7	62.8	87.7	136.9	221.7	411.5	720.2	1341.7	
32	74.3	84.7	106.5	148.6	233.4	403.0	711.6	1333.1	2540.9	
64	135.6	154.7	193.8	270.4	424.3	733.0	1350.6	2524.6	4889.6	

Table 2B

Use the ROM Calculator (“CSS\_ROM\_C3X.xls”) to determine actual X, Y dimensions, including non-binary configurations.