CSS NVM

NV Register – High Density Version (C5 Process)

CSS Nonvolatile Memory Library

General Description

This EEPROM is an N bit, nonvolatile register. It is implemented with CSS's High Density NV Latch cell. This NV Latch features a novel, high voltage level shifter to significantly reduce the area required by the cell. A margin test mode is included for better testability. It may also include redundant EE cells for improved reliability. Numerous serial and parallel interface options for entering data and reading out the contents of the NV register are provided. With the differential version of the NV Latch, once it has been programmed, valid data is available immediately after power-up.

Features

- Ultra Low Power and Wide Supply Range
- Memory Architecture:
  - Memory Size = 8 to 64 bits
  - Four NV Latch Cell Types (Single Ended/Differential, Redundant/Non-Redundant)
  - Numerous Serial and Parallel I/O Configurations Available
- Operating Modes:
  - Low Power Standby Mode (junction leakage only)
  - No Static Power in Read Mode (differential version)
  - Data Out is valid at power up (differential version)
- Tri-State Output Drivers
- Compatible with all C5, Double Poly processes

NV Latch Cell Features (Read Mode)

	EE Cell Architecture		Read Mode Characteristics					
Cell Name	EE Cell	Redundant?	NVOUT Valid If	Minimum VDD	Maximum VDD	Static Current	Access Time	Output Driver
NVL_SE3_HD	Single Ended	No	CE = 1	1.25V	5.5V	$I_{REF}/4$	< 50ns	Tri-State
NVL_SER3_HD	Single Ended	Yes	CE = 1	1.25V	5.5V	$I_{REF}/4$	< 50ns	Tri-State
NVL_CC3_HD	Differential	No	VDD > 1.25V	1.25V	5.5V	~ 0	< 10ns	Tri-State
NVL_CCR3_HD	Differential	Yes	VDD > 1.25V	1.25V	5.5V	~ 0	< 10ns	Tri-State

Table 1A

NV Latch Cell Features (Program Mode)

Cell Name	HV Cycles To Program	VDDmin	VDDmax	Static Current	Program Time	Maximum Program Cycles	Data Retention
NVL_SE3_HD	Erase + Write	1.5V	5.5V	~ 0	10ms	> 100K	> 10 years at 100°C
NVL_SER3_HD	Erase + Write	1.5V	5.5V	~ 0	10ms	> 100K	> 10 years at 100°C
NVL_CC3_HD	Erase + Write	1.5V	5.5V	~ 0	10ms	> 10K	> 10 years at 100°C
NVL_CCR3_HD	Erase + Write	1.5V	5.5V	~ 0	10ms	> 100K	> 10 years at 100°C

Table 1B

Specifications

Process: All AMI C5 processes except C5A & C5B (requires double Poly)
Temperature range: -40°C to +85°C
Supply Voltage Range:
Read = 1.25V to 5.5V
Program = 1.5V to 5.5V
Supply Current:
Read current ≈ 0 (differential version, after initial programming cycle)
Store current ≈ 0
Memory architecture: 8 to 64 parallel bits
Read Mode:
Synchronous (Single ended version)
Asynchronous (Differential version)
Store Mode:
VPP (≈ +20V) required for programming (typically supplied by a VPP Generator cell)
Store time ≈ 10 msec
Endurance (number of Store cycles) > 10K
Data Retention > 10 years at 100°C
Data I/O:
Core memory cell = N parallel Data Inputs, N parallel tri-state Data Outputs
Various serial and parallel I/O configurations are available (see Data I/O examples on pages 9 & 10)
IBias Requirements: I_{REF} ≈ 0.3µA ±25% (typically supplied by a VPP Generator cell)

Pin Descriptions

Power Pins

VDD	Positive supply voltage.
VSS	Ground.

Control Pins

CE	Enables Read & Program modes. Low current standby mode if low. (Active high.)
READ	Enables the Read & Margin Read modes. (Active high.)
PROG	Enables the Erase & Write programming modes. (Active high.)
E/WB	Selects between Erase & Write modes. (Low = Write, High = Erase.)
MRGN	Enables Margin test mode. (Active high.)
ERASE_S	Enables the Erase mode. (Active high, +20V.)
WRITE_S	Enables the Write mode. (Active high, +20V.)

Data I/O Pins

DIN[N:0]	Data input lines, 8 to 64 total. Provides data to be programmed into the NV Latches.
NVOUT[N:0]	Nonvolatile data output lines, 8 to 64 total.
OE	Enables the tri-state output drivers. (Active high)
IMRGN	Test current when Margin Mode is active. (Sink to VSS)
MFAIL	Margin test result (a digital output – a logic one indicates that one or more bits failed the margin test).

Operating Modes

Standby: Output drivers are tri-stated. (Low current mode for single ended version.)

Read: Data Out equals NVOUT, last programmed value.

Margin: Allows indirect check of the EE Cell V_T. Test result indicated by state of MFAIL signal. The IMRGN pin is active and sets the amount of margin (how strongly the EE cell must be programmed to pass this test.)

Erase: Programs all EE cell floating gate devices to depletion. (N_{CH} V_T < 0V.)

Write: Programs the appropriate EE cells (depending on DIN) to an "OFF" state.

A summary of the operating modes is provided in Table 2.

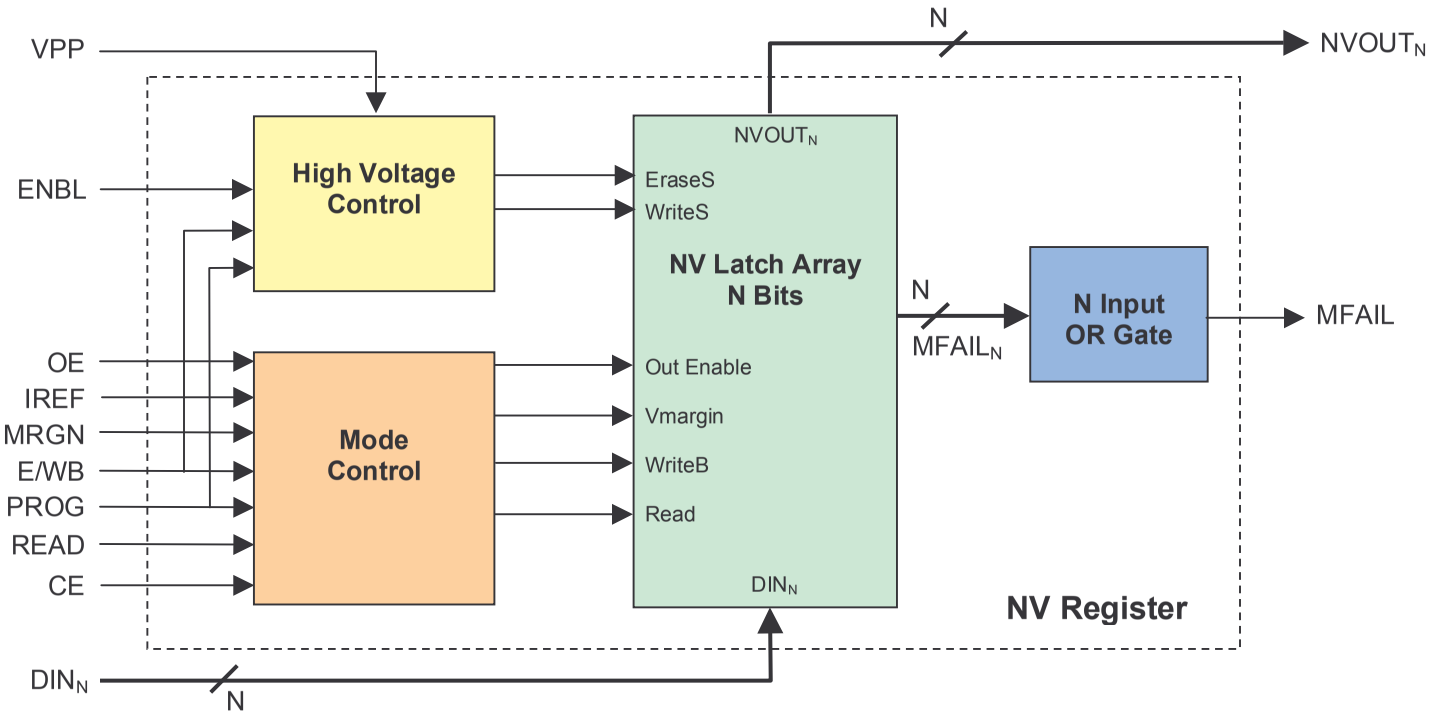
Operating Mode Table

Mode	Description	CE	READ	PROG	E/WB	OE	IMRGN	MFAIL	DIN_N	$NVOUT_N$
Standby	Low Current Mode	0	X	X	X	0 1	X	1	X	High Z 0
Read	Read Mode	1	1	X	X	1	X	1	X	NV Out_N
Margin	Check EE Cell Margin	1	1	X	X	1	I_M	0 = Pass	X	NV Out_N
Erase	Clear all EE Cells (Note 1)	1	0	1	1	0 1	X	1	X	High Z 0
Write	Write NV Data	1	0	1	0	0 1	X	1	Valid	High Z 0

Table 2

Notes:
1) **IMPORTANT!** – After an Erase cycle, the state of the differential NV Latch is indeterminate until a Write has been performed.

NV Register Block Diagram

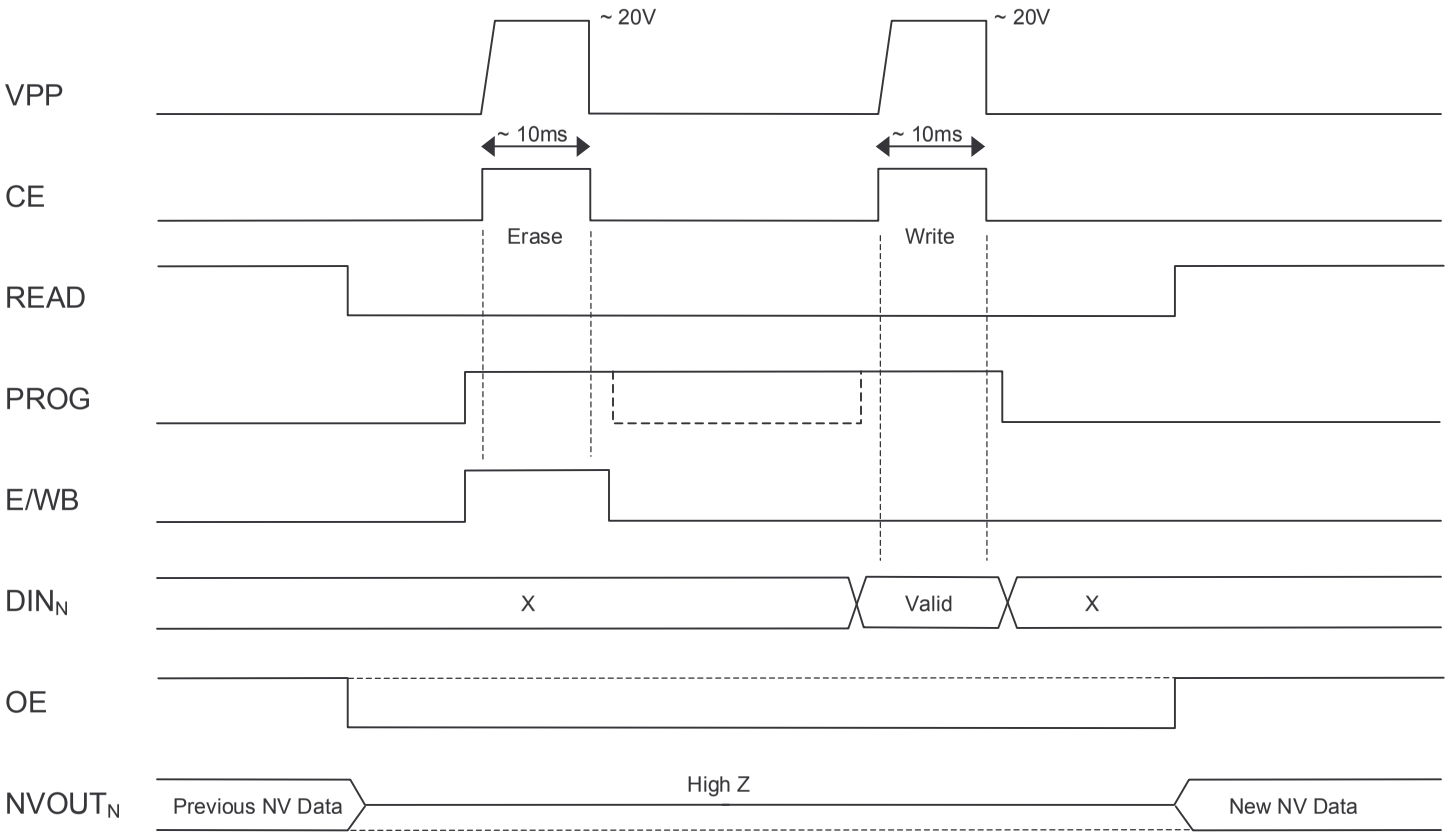


Block Diagram 1

Timing Diagrams

Program NV Memory (Erase & Write)

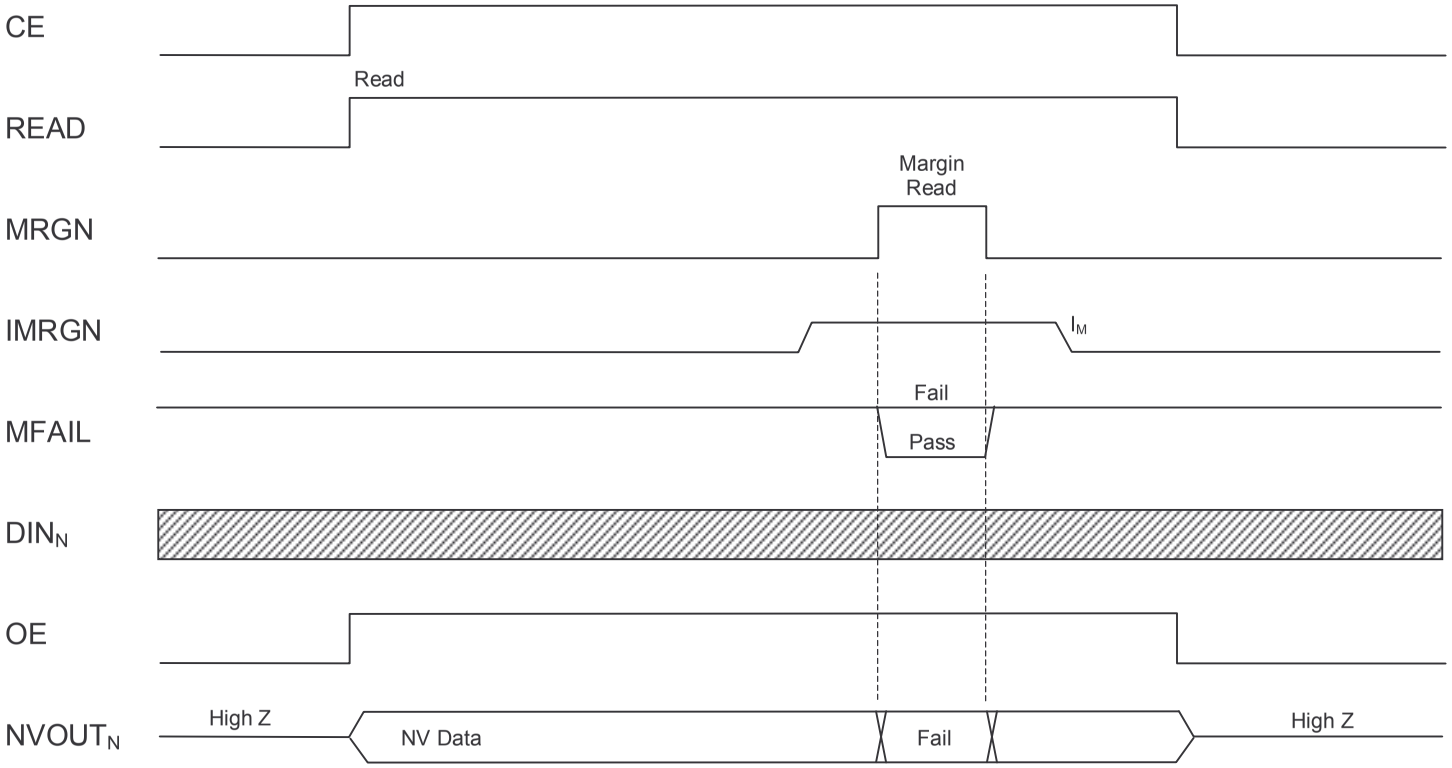
(MRGN = 0, IREF = X)



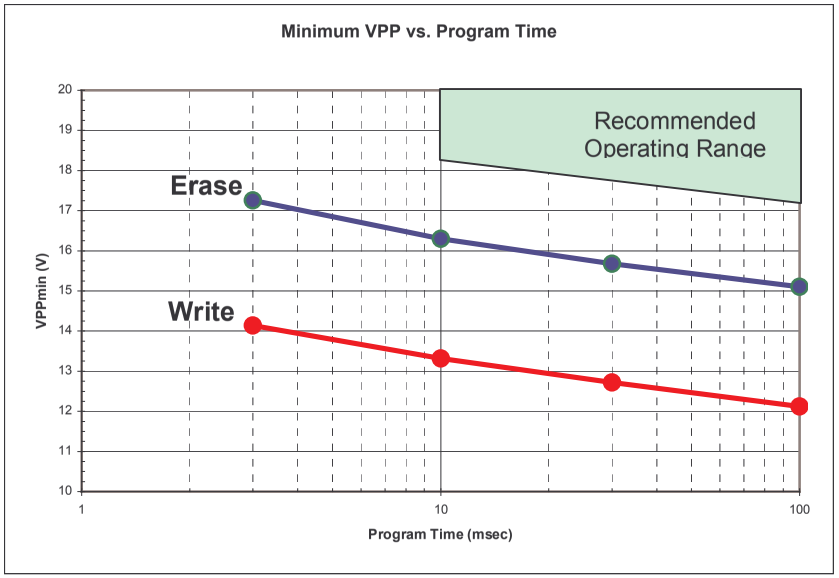
Timing Diagrams

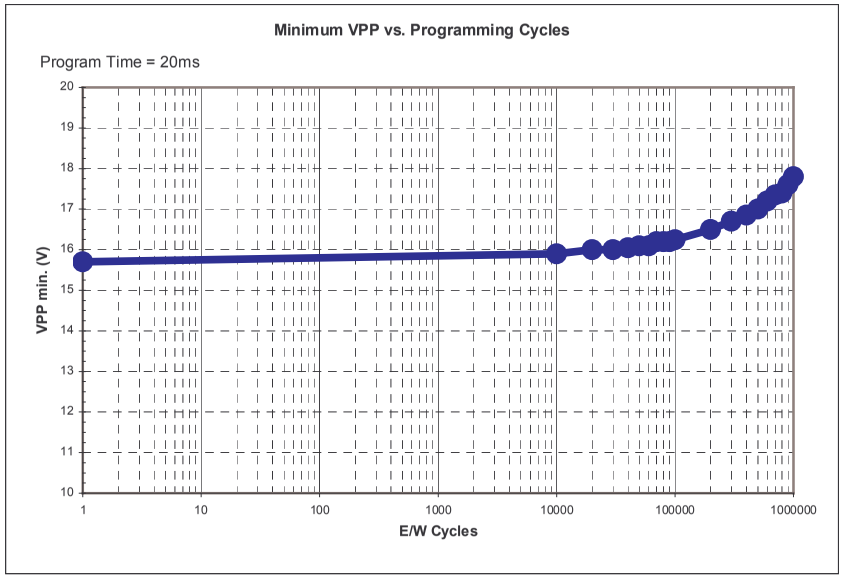
Enable NVOUT & Read, Read with Margin

(PROG = X, E/WB = X)



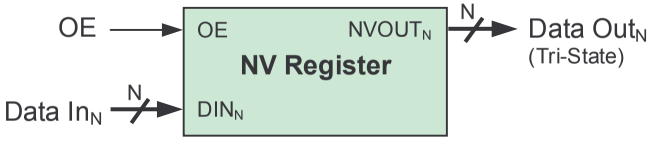
Electrical Characteristics (Typical)



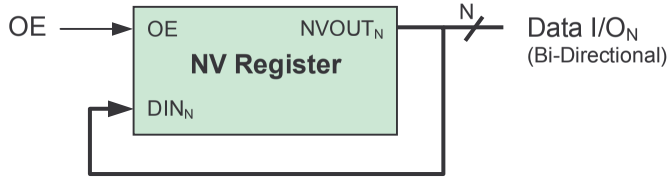


Typical Data I/O Configurations

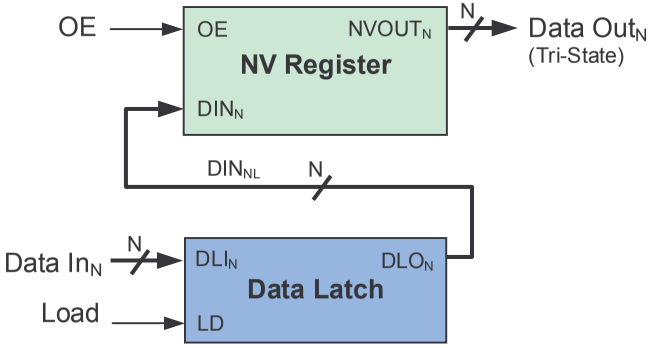
Type A
N Parallel Inputs
N Parallel Tri-State Outputs



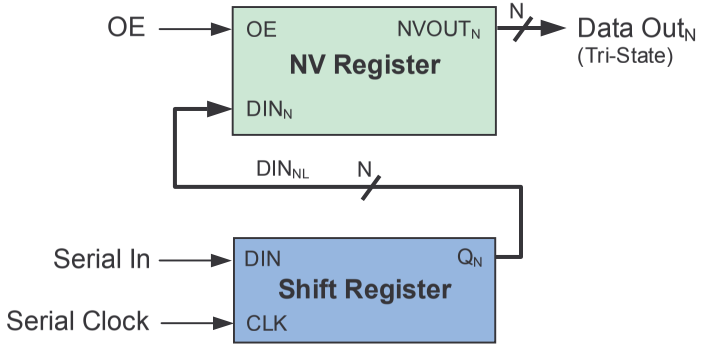
Type B
N Parallel Bi-Directional I/O's



Type C
N Parallel Latched Inputs
N Parallel Tri-State Outputs

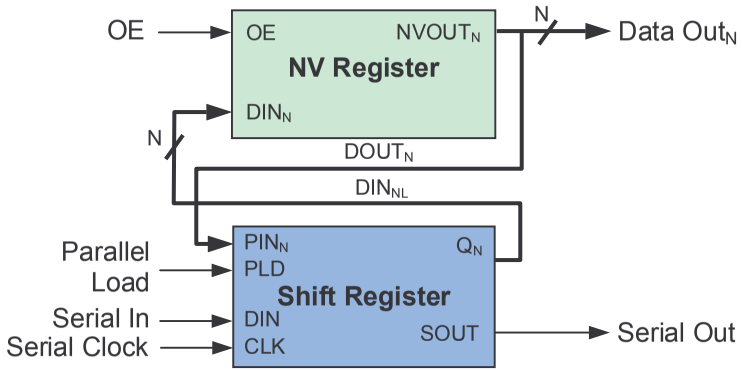


Type D
1 Serial Input
N Parallel Tri-State Outputs

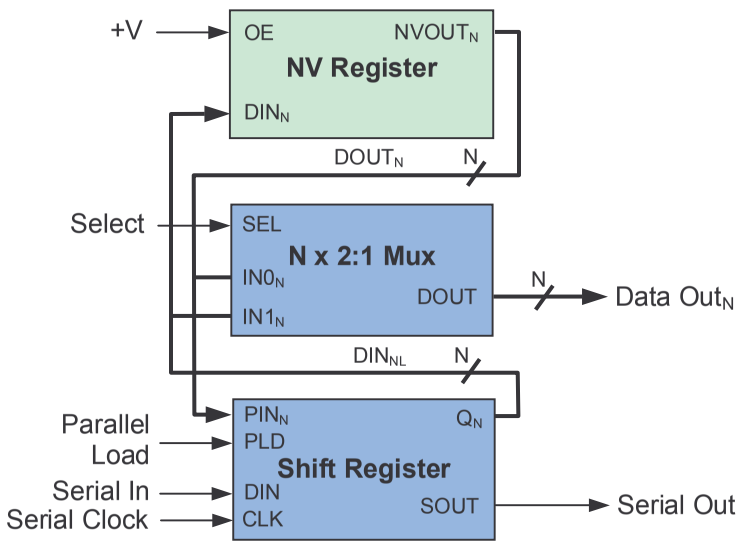


Block Diagrams 2A, 2B, 2C & 2D

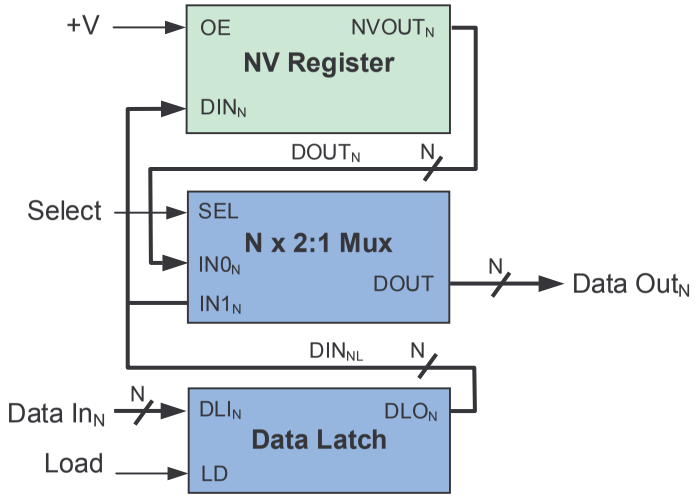
Type E
1 Serial Input, 1 Serial Output
N Parallel Tri-State Outputs



Type F
1 Serial Input, 1 Serial Output
N Parallel Multiplexed Outputs



Type G
N Parallel Latched Inputs
N Parallel Multiplexed Outputs



Block Diagrams 2E, 2F & 2G

Data I/O Interface Features

Type	Data Inputs & Outputs	DIN must be valid during:	Value of DOUT during Store cycle	Transparent Mode? (DOUT = DIN)	Serial Readout of NVOUT?	Tri-State Output?
A	N Parallel Inputs N Parallel Tri-State Outputs	Entire Store Cycle	1 or High Z	No	No	Yes
B	N Parallel Bi-Directional I/o's	Entire Store Cycle	DIN	No	No	Yes
C	N Parallel Latched Inputs N Parallel Tri-State Outputs	Falling Edge of Load	1 or High Z	No	No	Yes
D	1 Serial Input N Parallel Tri-State Outputs	Rising Edge of SCLK	1 or High Z	No	No	Yes
E	1 Serial Input, 1 Serial Output N Parallel Tri-State Outputs	Rising Edge of SCLK	1 or High Z	No	Yes	Yes
F	1 Serial Input, 1 Serial Output N Multiplexed Outputs	Rising Edge of SCLK	Latched DIN or 1	Yes	Yes	No
G	N Parallel Latched Inputs N Multiplexed Outputs	Falling Edge of Load	Latched DIN or 1	Yes	No	No

Table 3

NV Register Area for Typical Memory & Data I/O Configurations

NV Latch Type = Single Ended

I/O Configuration			Redundant EE Cell?	NV Register Area (K sq. um) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	4.0	7.0	13.0	24.9
B	N Parallel Bi-Directional I/O's		No	4.0	7.0	13.0	24.9
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	5.5	9.5	17.7	34.0
B	N Parallel Bi-Directional I/O's		Yes	5.5	9.5	17.7	34.0

Table 4A

NV Latch Type = Differential

I/O Configuration			Redundant EE Cell?	NV Register Area (K sq. um) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	9.4	16.3	30.3	58.1
B	N Parallel Bi-Directional I/O's		No	9.4	16.3	30.3	58.1
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	No	11.7	20.4	37.9	72.8
D	1 Serial Input	N Parallel Tri-State Outputs	No	10.9	20.1	38.7	75.7
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	No	13.1	22.9	42.4	81.5
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	No	19.9	36.8	70.8	138.6
G	N Parallel Latched Inputs	N Multiplexed Outputs	No	(18*)	(34*)	(65*)	(127*)
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	13.8	24.0	44.5	85.5
B	N Parallel Bi-Directional I/O's		Yes	13.8	24.0	44.5	85.5
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	Yes	16.1	28.1	52.1	100.1
D	1 Serial Input	N Parallel Tri-State Outputs	Yes	14.7	27.2	52.3	102.5
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	Yes	17.5	30.6	56.6	108.8
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	Yes	23.7	44.0	84.4	165.4
G	N Parallel Latched Inputs	N Multiplexed Outputs	Yes	22.0	40.8	78.4	153.6

(*) = Estimated

Table 4B

NV Register Area for Typical Memory & Data I/O Configurations

NV Latch Type = Single Ended

I/O Configuration			Redundant EE Cell?	NV Register Area (sq. mils) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	6.2	10.9	20.1	38.6
B	N Parallel Bi-Directional I/O's		No	6.2	10.9	20.1	38.6
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	8.5	14.8	27.4	52.7
B	N Parallel Bi-Directional I/O's		Yes	8.5	14.8	27.4	52.7

Table 5A

NV Latch Type = Cross-Coupled

I/O Configuration			Redundant EE Cell?	NV Register Area (sq. mils) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	14.5	25.3	46.9	90.1
B	N Parallel Bi-Directional I/O's		No	14.5	25.3	46.9	90.1
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	No	18.2	31.7	58.7	112.8
D	1 Serial Input	N Parallel Tri-State Outputs	No	16.8	31.2	59.9	117.4
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	No	20.3	35.5	65.7	126.3
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	No	30.8	57.1	109.7	214.9
G	N Parallel Latched Inputs	N Multiplexed Outputs	No	(28*)	(52*)	(100*)	(197*)
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	21.3	37.2	69.0	132.5
B	N Parallel Bi-Directional I/O's		Yes	21.3	37.2	69.0	132.5
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	Yes	25.0	43.6	80.8	155.2
D	1 Serial Input	N Parallel Tri-State Outputs	Yes	22.8	42.2	81.1	158.9
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	Yes	27.2	47.4	87.8	168.7
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	Yes	36.8	68.2	130.9	256.4
G	N Parallel Latched Inputs	N Multiplexed Outputs	Yes	34.2	63.3	121.6	238.1

(*) = Estimated

Table 5B