CSS NVM — EEPROM Application Note #1 – Test Modes

CSS Nonvolatile Memory Library

Test Modes

Two special test modes have been included to provide a means to insure the integrity of the nonvolatile data. The "Margin" test mode allows the current used to sense the state of the EE cell to be increased or decreased. This test can be used to insure that there is an adequate threshold shift in the EE cell to read correctly. The second test mode provides direct access to the EE cell current.

The Margin test is intended to be used as part of a production screen, to provide added assurance that the EE cells are programming adequately. If performed as a "Go – No Go" test using one Margin current level, it adds very little to the total test time. The EE cell current measurement is relatively slow and intended for device characterization, particularly EEPROM retention.

Margin Test Mode

The Margin test mode is entered by taking the MRGN_EN input high while in Read mode. The Margin mode enables the I_MRGN input, an analog current input to the Bias Current Generator for the sense amps. (Please refer to Table #1, Block Diagram #1 and the Timing Diagrams.) To increase the Read Sense current, "I_{RS}", used in the sense amplifier, a small current, "I_M", is sunk from the I_MRGN pin to VSS. Increasing I_{RS} makes it more difficult to read a bit written to a logic one. Conversely, sourcing a small current from VDD into the I_MRGN pin, decreases I_{RS} and makes it more difficult to read an erased bit (logic zero).

A typical "Go – No Go" Margin test sequence might be:

1) Measure internal Read Sense current level by forcing I_MRGN to VDD and measuring I_{RS} (to VSS)
2) Erase all bits to "0"
3) Read all bits without Margin (verify normal Read)
4) Enable the Margin mode, enable I_M source (~ ½ x I_{RS}, typically several microamps) and re-read all bits
5) Write all bits to "1"
6) Read all bits without Margin (verify normal Read)
7) Enable the Margin mode, enable I_M sink (~½ x I_{RS}, typically several microamps) and re-read all bits

To characterize the pass/fail point for each bit, repeat steps #1 through #6, while increasing I_M. (Wait at least 10us between changing I_M and reading the memory to allow the Bias Current Generator to settle.)

Note – A full functional test for the EEPROM should also include checkerboard and random patterns to identify near neighbor and decoder defects.

EE Cell Current Measurement

A second special test mode allows the cell current, I_{EE}, of each EE bit to be measured directly. This operating mode is enabled by taking the TM_EN input high while in the Margin Read mode. Entering this test mode enables an analog switch between the output of the Column Mux and the $DOUT_N$ pin. The I_MRGN input must be tied to VDD to force the Read Bias Current to zero and OE must be held low (inactive) to tri-state the DOUT driver. (Please refer to Table #1, Block Diagram #1 and the Timing Diagrams.)

Note: To utilize this test mode, an analog signal path from $DOUT_N$ to an external pin must be provided. (Nch only is OK.)

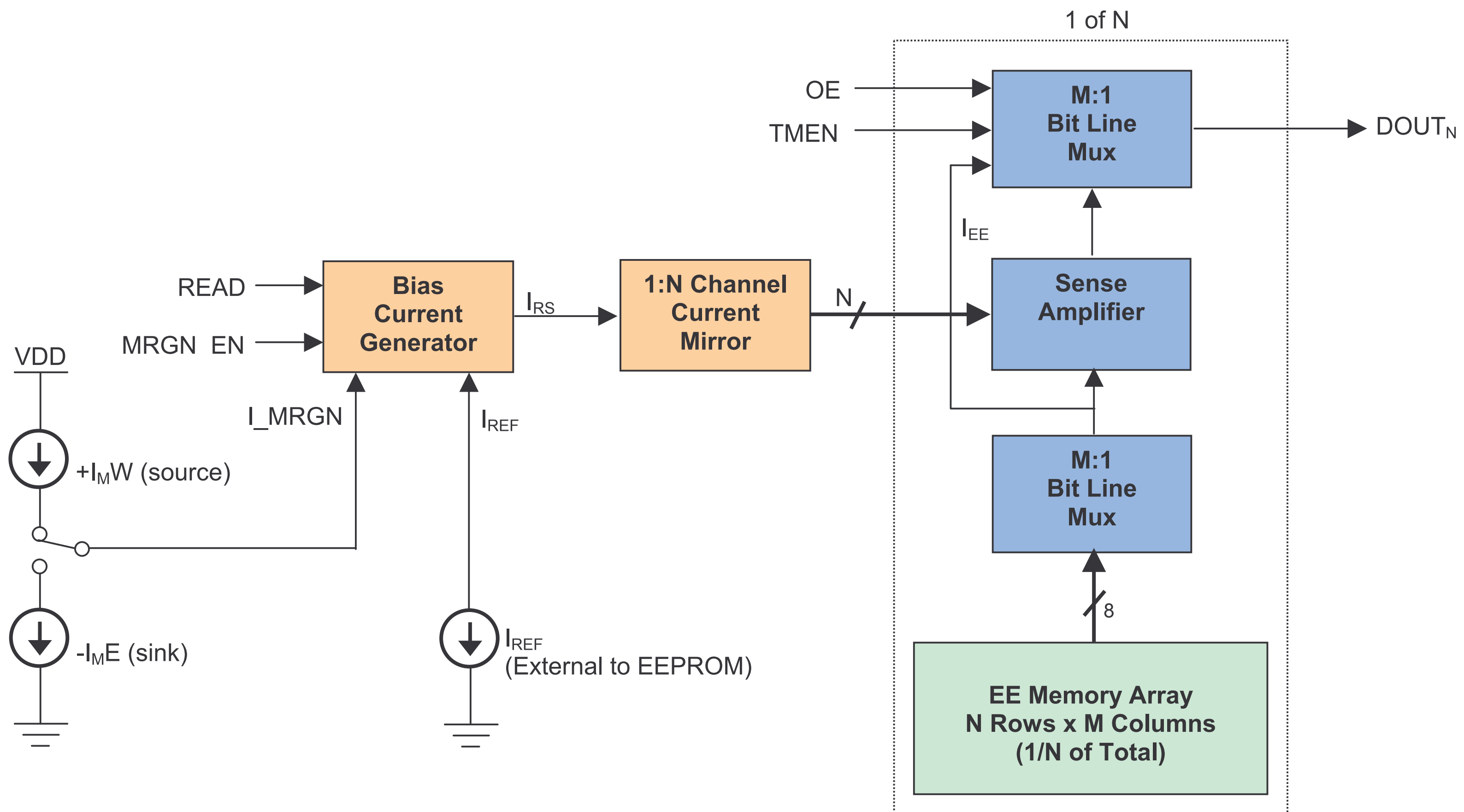
Read Modes

PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don’t Care, DIN = Don’t Care

Mode	Description	CE	READ	OE	MRGN_EN	TMEN	I_MRGN	$ADDRESS_N$	$DOUT_N$
Standby	Low Current Standby	0	0	0	0	0	X	X	High Z
Read	Normal Read Mode	1	1	1	0	0	X	Valid	$DOUT_N$
MarginE Read	Read with Margin (Erased state)	1	1	1	1	0	$+I_M$ (source)	Valid	0 = Pass
MarginW Read	Read with Margin (Written state)	1	1	1	1	0	$- I_M$ (sink)	Valid	1 = Pass
Test Mode	Measure EE Cell Current	1	1	0	1	1	VDD	Valid	I_{EE} Cell

Table 1

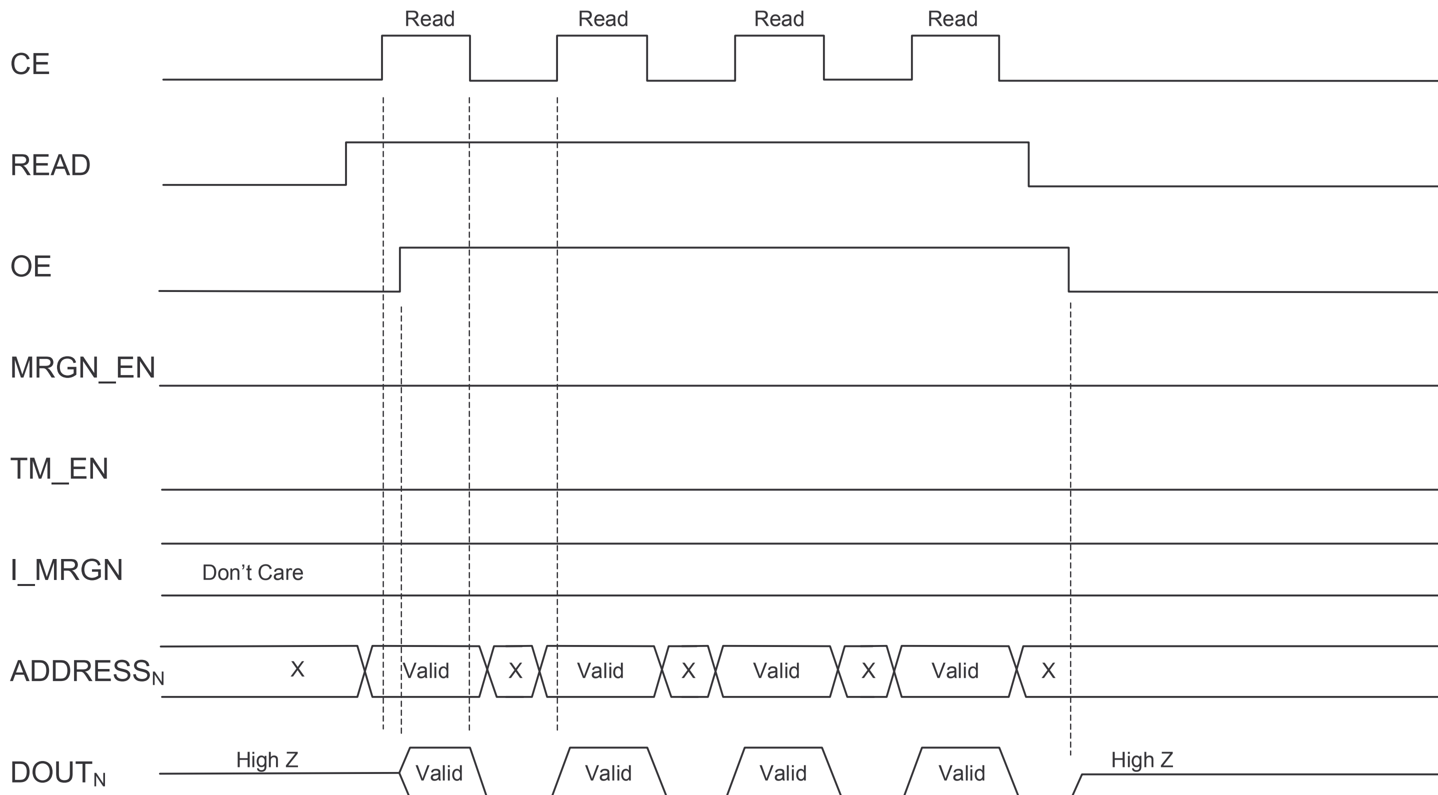
Test Mode Block Diagram



Block Diagram 1

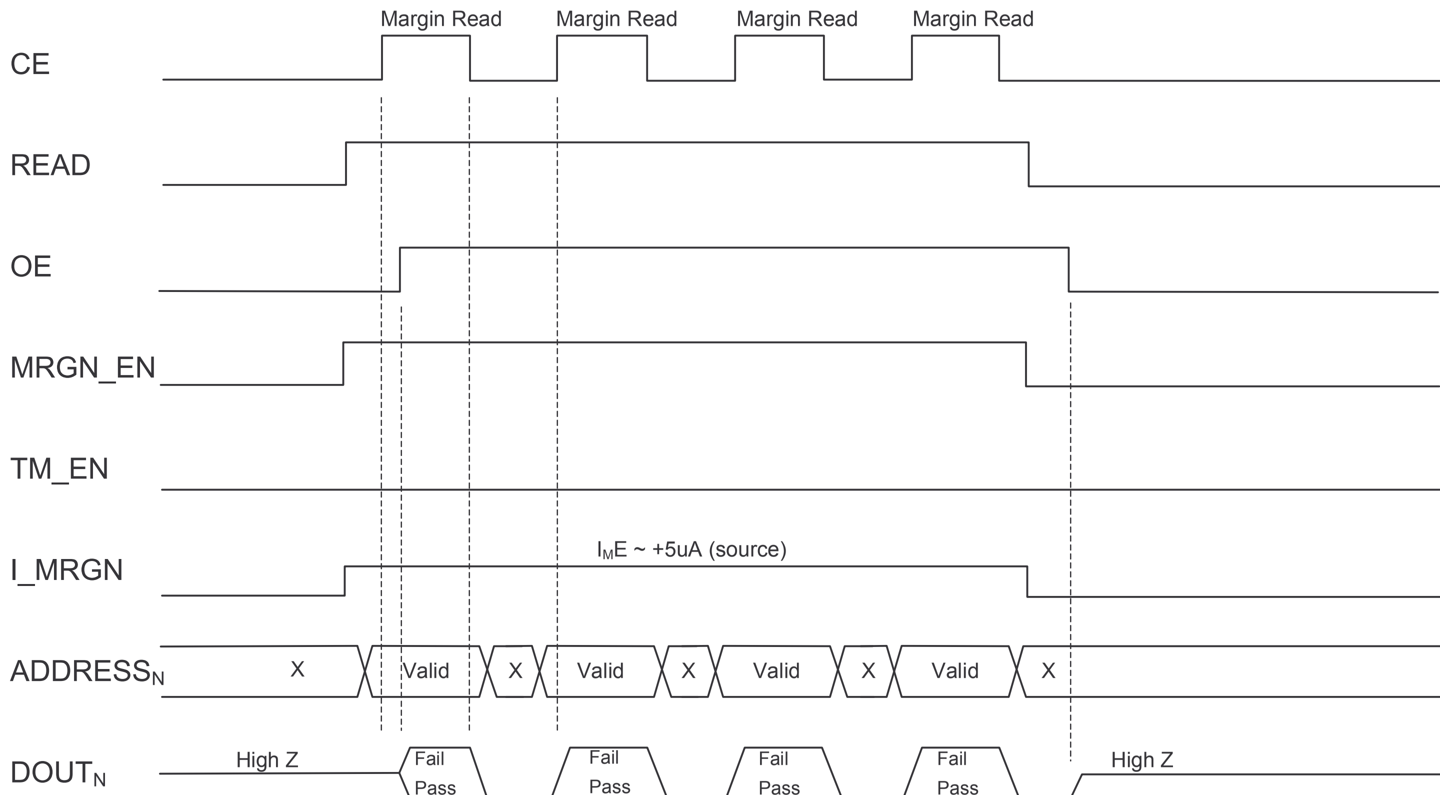
Timing Diagrams

Read (Normal)
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



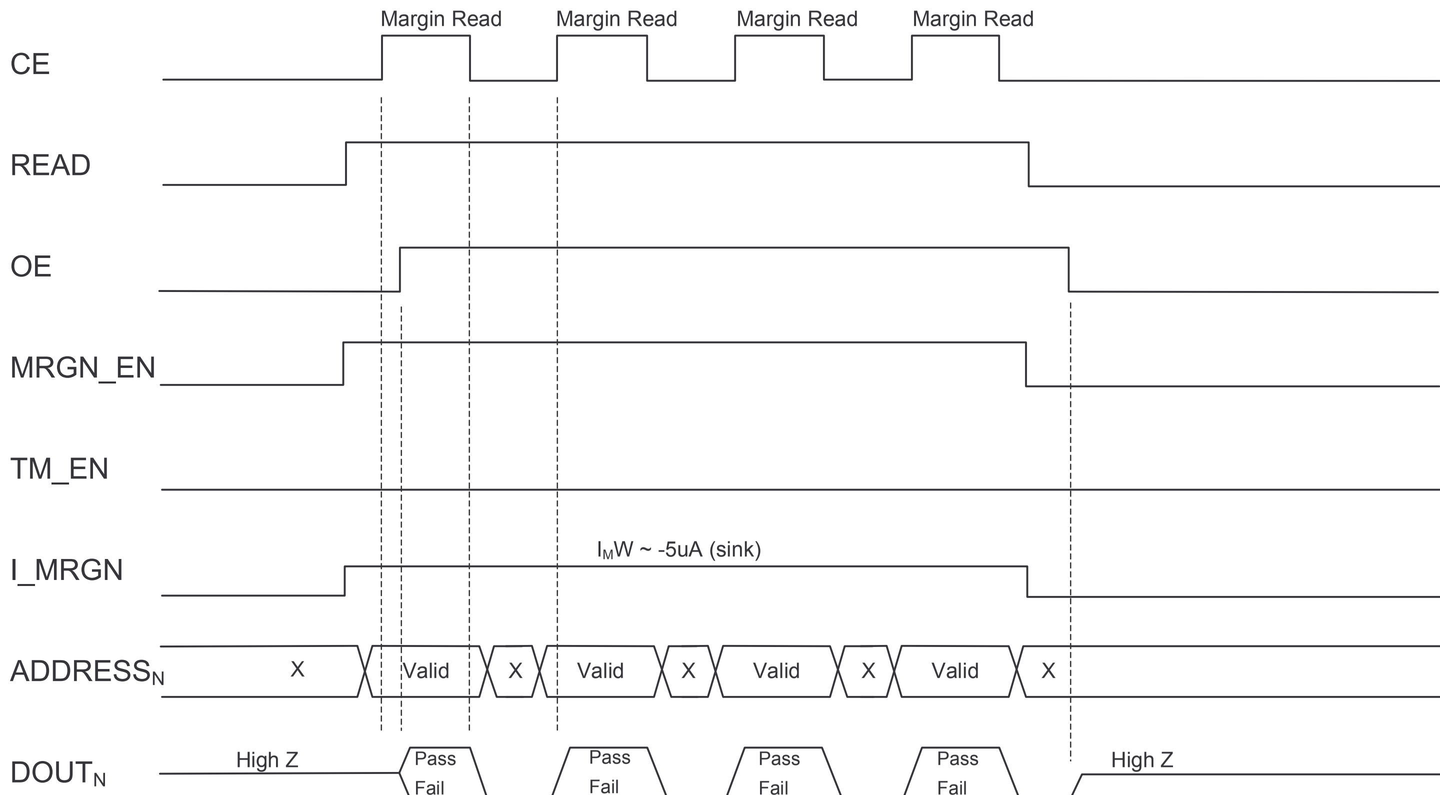
Timing Diagrams

Read with Margin (Erased Bits)
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



Timing Diagrams

Read with Margin (Written Bits)
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



Timing Diagrams

Measure EE Cell Current

PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don’t Care, DIN = Don’t Care