CSS NVM

NV Register - *Classic* Version (C5 Process)

CSS Nonvolatile Memory Library

General Description

This EEPROM is an N bit, nonvolatile register. It is implemented with CSS's *Classic* NV Latch cell. This NV Latch features a single cycle store operation for faster programming. A margin test mode is included for better testability. It may also include redundant EE cells for improved reliability. Numerous serial and parallel interface options for entering data and reading out the contents of the NV register are provided. With the differential version of the NV Latch, once it has been programmed, valid data is available immediately after power-up.

Features

- Ultra Low Power and Wide Supply Range
- Memory Architecture:
  - Memory Size = 8 to 64 bits
  - Three NV Latch Cell Types (Single Ended/Differential, Redundant/Non-Redundant)
  - Numerous Serial and Parallel I/O Configurations Available
- Operating Modes:
  - Low Power Standby Mode (junction leakage only)
  - No Static Power in Read Mode (differential version)
  - Data Out is valid at power up (differential version)
  - Single Cycle Store Mode (No erase cycle required)
- Output Drivers:
  - Tri-State for buss architectures
- Compatible with all C5, Double Poly processes
  - Does NOT require 1K Poly or Metal3

NV Latch Cell Features (Read Mode)

	EE Cell Architecture		Read Mode Characteristics					
Cell Name	EE Cell	Redundant?	NVOUT Valid If	Minimum VDD	Maximum VDD	Static Current	Access Time	Output Driver
NVL_SER3	Single Ended	Yes	CE = 1	1.25V	5.5V	$I_{REF}/4$	< 50ns	Tri-State
NVL_CC3	Differential	No	VDD > 1.25V	1.25V	5.5V	~ 0	< 10ns	Tri-State
NVL_CCR3	Differential	Yes	VDD > 1.25V	1.25V	5.5V	~ 0	< 10ns	Tri-State

Table 1A

NV Latch Cell Features (Program Mode)

Cell Name	HV Cycles To Program	VDDmin	VDDmax	Static Current	Program Time	Maximum Program Cycles	Data Retention
NVL_SER3	1 (Store)	1.25V	5.5V	~ 0	10ms	> 100K	> 10 years at 100°C
NVL_CC3	1 (Store)	1.25V	5.5V	~ 0	10ms	> 10K	> 10 years at 100°C
NVL_CCR3	1 (Store)	1.25V	5.5V	~ 0	10ms	> 100K	> 10 years at 100°C

Table 1B

Specifications

Process: All AMI C5 processes except C5A & C5B (requires double Poly)
Temperature range: -40°C to +85°C
Supply Voltage: 1.25V to 5.5V
Supply Current:
- Read current (differential version) ≈ 0 (after initial programming cycle)
- Read current (single ended version) ≈ $I_{REF/4}$ (per bit)
- Store current ≈ 0.15µA (drawn by HV control circuit, one per NV Register)

Memory architecture: 8 to 64 parallel bits
Read Mode:
- Synchronous (Single ended version)
- Asynchronous – data always valid except during programming (Differential version)

Store Mode:
- VPP (≈ +20V) required for programming (typically supplied by a VPP Generator cell)
- Store time ≈ 10 msec
- Endurance (number of Store cycles) > 10K
- Data Retention > 50 years at 100°C

Data I/O:
- Core memory cell = N parallel Data Inputs, N parallel tri-state Data Outputs
- Numerous serial and parallel I/O configurations are available (see Data I/O examples on pages 8 & 9)

IBias Requirements: I_{REF} ≈ 0.3µA ±25% (typically supplied by a VPP Generator cell)

Pin Descriptions

Power Pins

VDD	Positive supply voltage.
VSS	Ground.
VPP	Programming voltage (from the VPP Generator, a separate block)

Control Pins

PROGB	Enables the Program mode. (Active low.)
OE	Enables the tri-state output drivers. (Active high)
MRGN_EN	Enables margin test mode. (Active high.)

Data I/O Pins

DIN[N:0]	Data input lines, 8 to 64 total. Provides data to be programmed into the NV Latches.
NVOUT[N:0]	Nonvolatile data output lines, 8 to 64 total.
MFAIL	Margin test result (a digital output – a logic one indicates that one or more bits failed the margin test).

Reference Pins

I_MRGN	Test current when Margin Mode is active. (Sink to VSS)
IBIAS	Reference current, used during Store mode only. (Typically supplied by VPP Generator.)

Operating Modes

(Shown for a differential NV Latch)

Standby: Output drivers are tri-stated. (Low current mode for single ended version.)

Read: Data Out equals NVOUT, last programmed value.

Margin: Allows indirect check of the EE Cell Vt. Test result indicated by state of MFAIL signal. The VMRGN pin is active and sets the amount of margin (how strongly the EE cell must be programmed to pass this test.)

Store: Programs all NV bits to the current value of DIN. (Done in one step. 1's change to 0's, 0's change to 1's, if appropriate.)

A summary of the operating modes is provided in Table 2.

Operating Mode Table

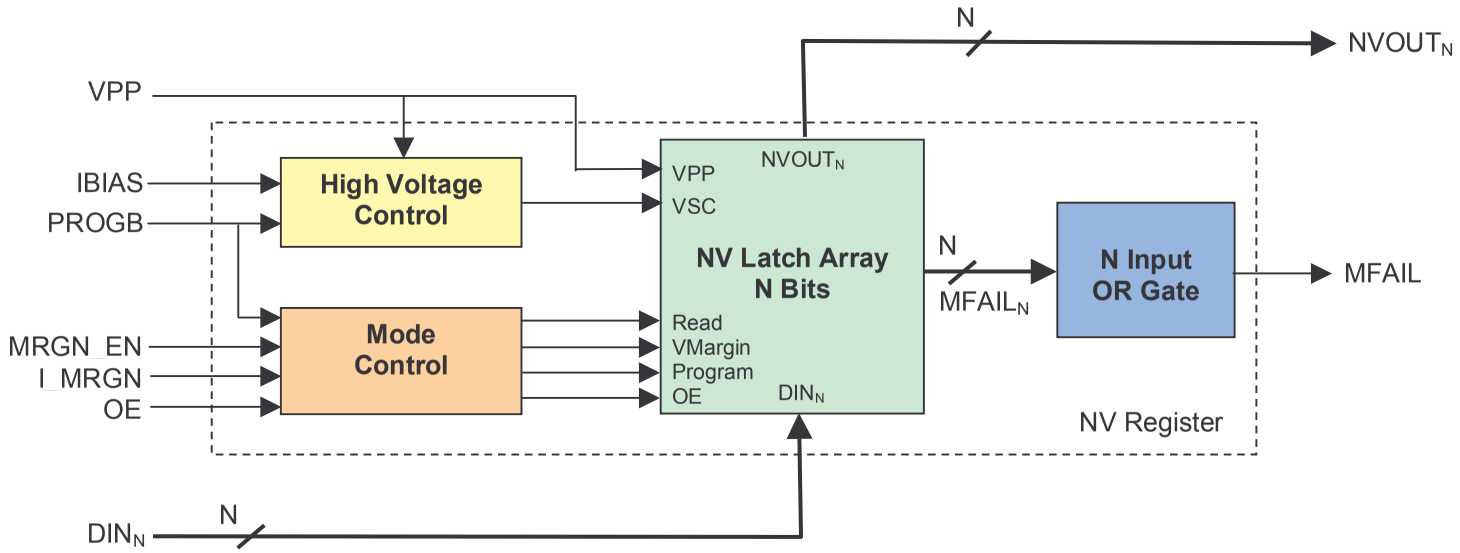
Mode	Description	OE	PROGB	MRGN_EN	I_MRGN	MFAIL	DIN_N	$NVOUT_N$
Standby	Read Mode, Output Disabled	0	1	0	Open	0	X	High Z
Read	Read Mode, Output Active	1	1	0	Open	0	X	NV Out_N
Margin	Check EE Cell Margin	1	1	1	I_{MRGN}	1 = Fail	X	NV Out_N
Store	Program NV Data	X	0	0	Open	0	Valid	1 or High Z

Table 2

Notes:

1) During Programming, if OE = 0, $NVOUT_N$ will be tri-stated. If OE = 1, $NVOUT_N$ will equal a logic one.
2) When Margin Mode is inactive, the I_MRGN pin should be open or pulled to VDD. (It is pulled to VDD by the Mode Control circuit.)

NV Register Block Diagram

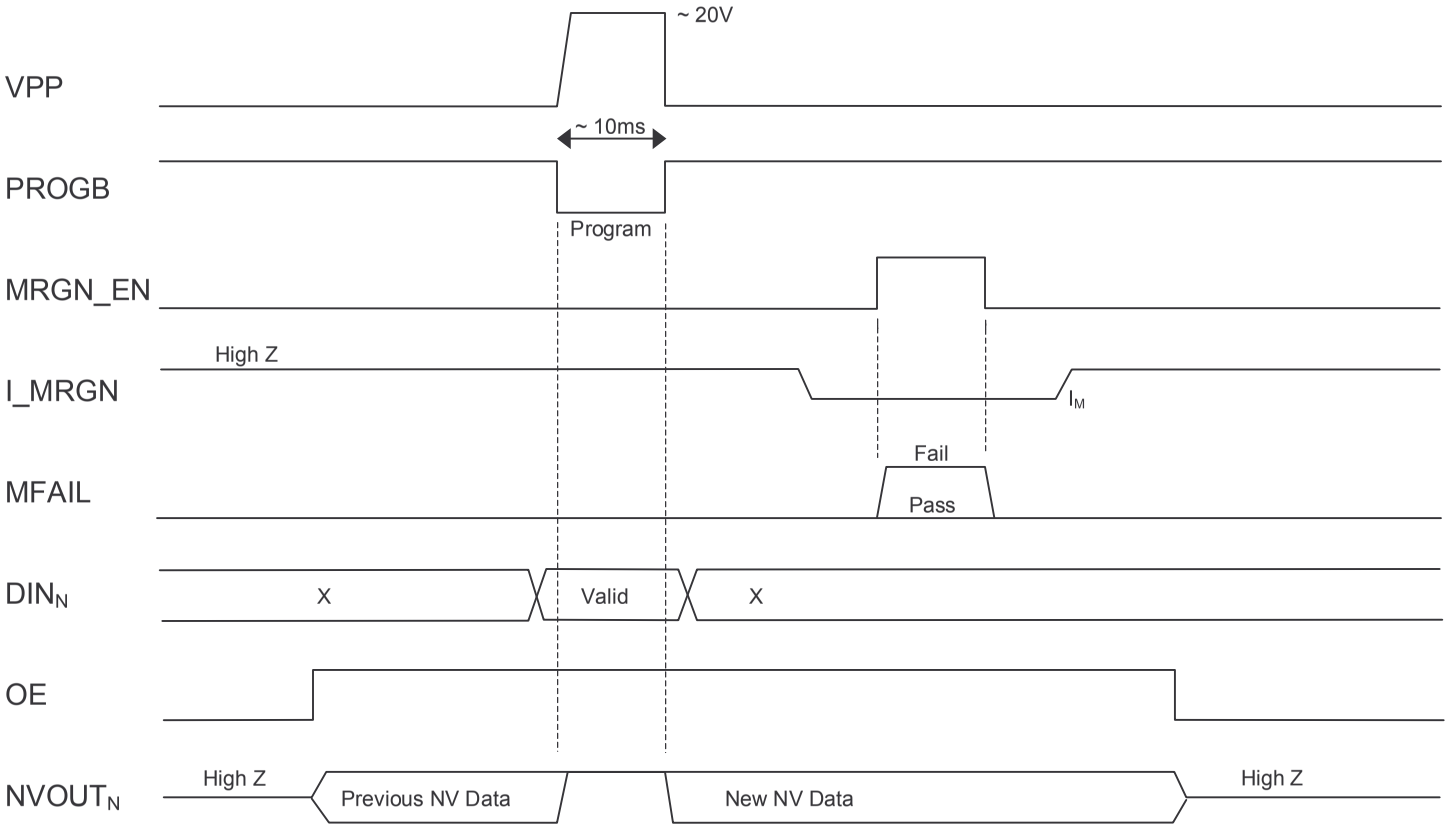


Block Diagram 1

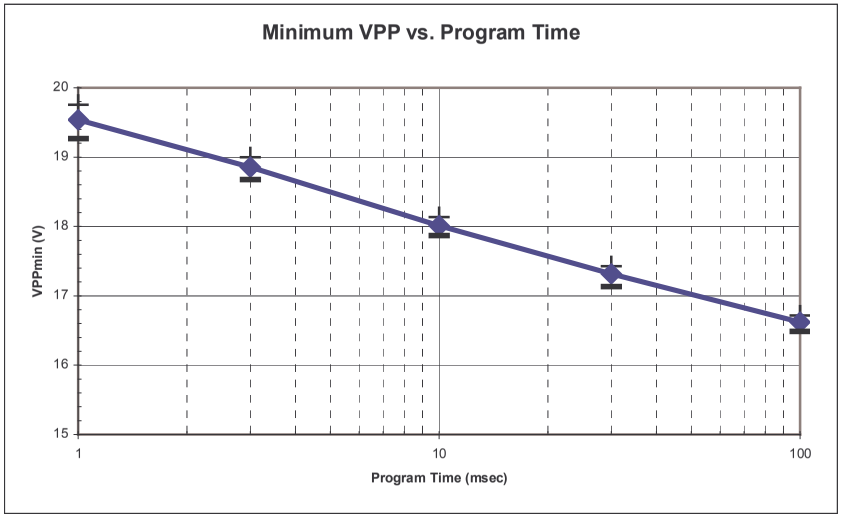
Timing Diagrams

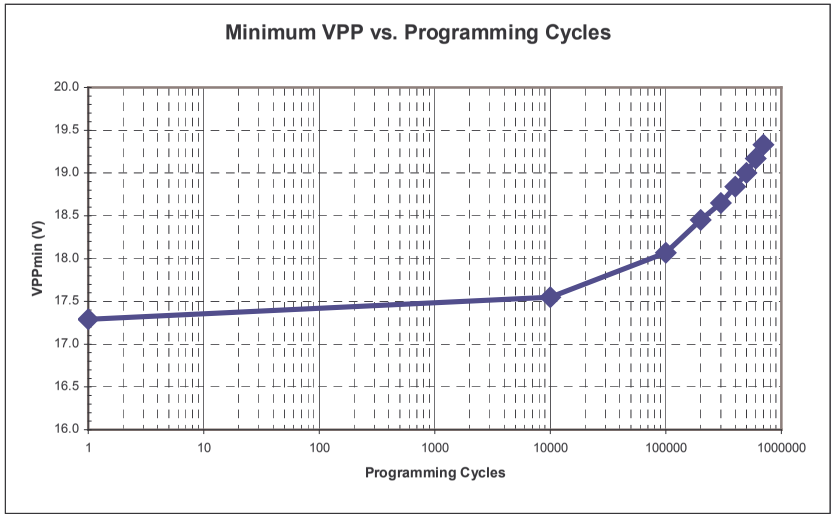
(Shown for a differential NV Latch)

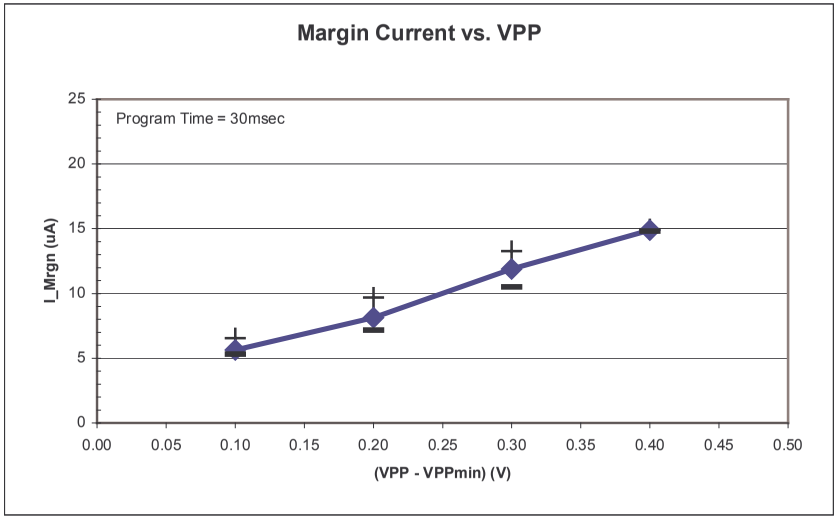
Enable NVOUT & Read, Program NV Memory, Read with Margin



Electrical Characteristics (Typical)

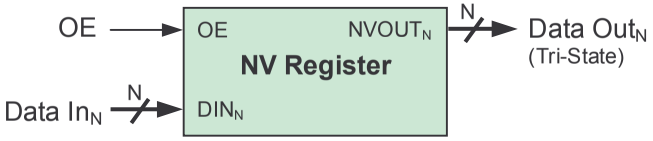




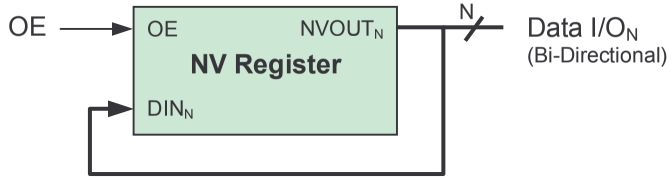


Typical Data I/O Configurations

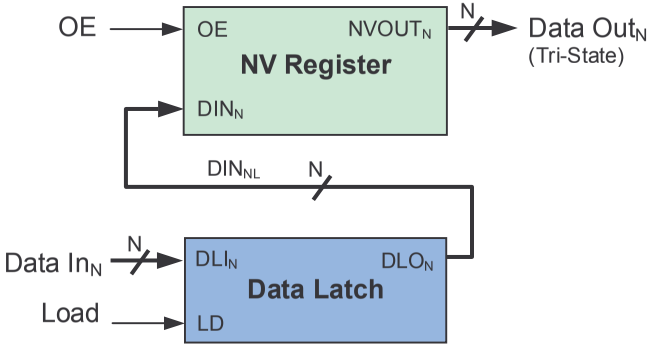
Type A
N Parallel Inputs
N Parallel Tri-State Outputs



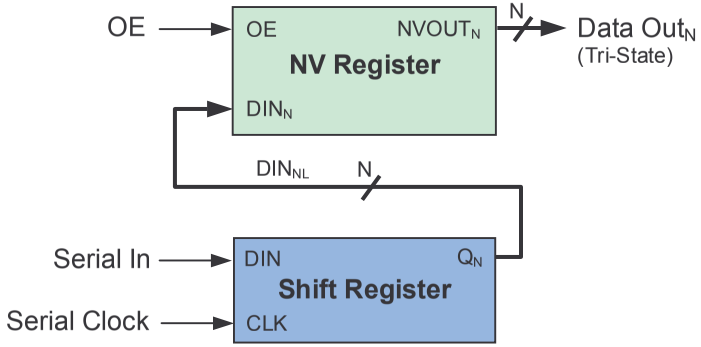
Type B
N Parallel Bi-Directional I/O's



Type C
N Parallel Latched Inputs
N Parallel Tri-State Outputs



Type D
1 Serial Input
N Parallel Tri-State Outputs



Block Diagrams 2A, 2B, 2C & 2D

NV Register - *Classic* Version (C5 Process)

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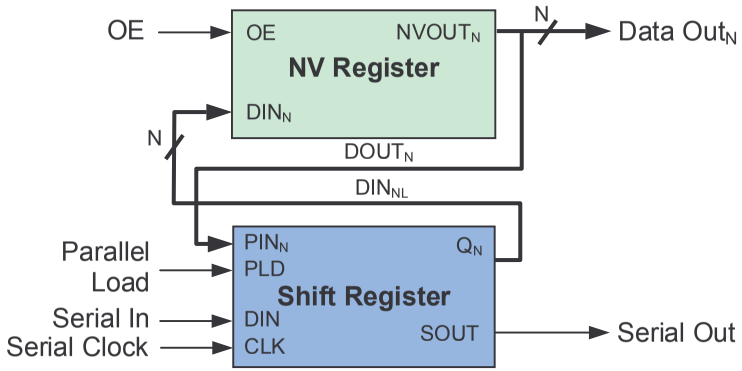
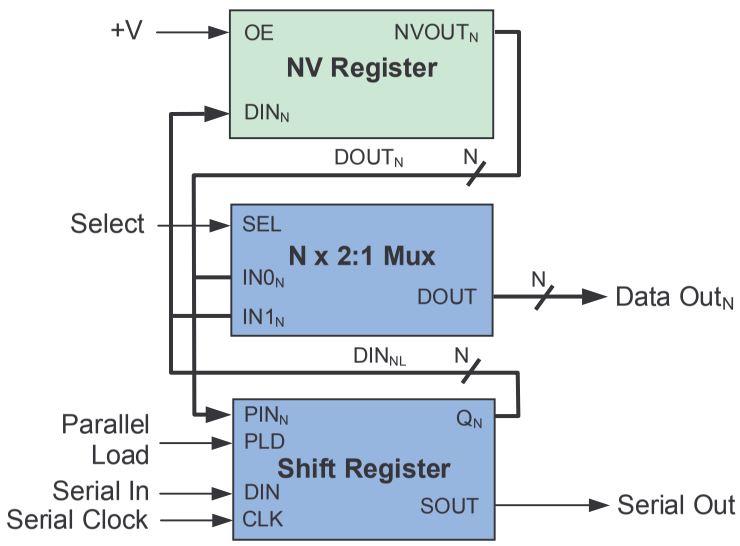
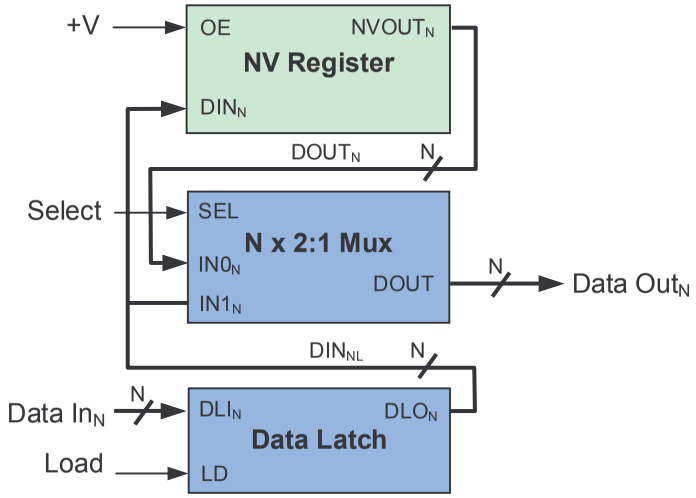
Type E
1 Serial Input, 1 Serial Output
N Parallel Tri-State Outputs



Type F
1 Serial Input, 1 Serial Output
N Parallel Multiplexed Outputs



Type G
N Parallel Latched Inputs
N Parallel Multiplexed Outputs



Block Diagrams 2E, 2F & 2G

Data I/O Interface Features

Type	Data Inputs & Outputs	DIN must be valid during:	Value of DOUT during Store cycle	Transparent Mode? (DOUT = DIN)	Serial Readout of NVOUT?	Tri-State Output?
A	N Parallel Inputs N Parallel Tri-State Outputs	Entire Store Cycle	1 or High Z	No	No	Yes
B	N Parallel Bi-Directional I/o's	Entire Store Cycle	DIN	No	No	Yes
C	N Parallel Latched Inputs N Parallel Tri-State Outputs	Falling Edge of Load	1 or High Z	No	No	Yes
D	1 Serial Input N Parallel Tri-State Outputs	Rising Edge of SCLK	1 or High Z	No	No	Yes
E	1 Serial Input, 1 Serial Output N Parallel Tri-State Outputs	Rising Edge of SCLK	1 or High Z	No	Yes	Yes
F	1 Serial Input, 1 Serial Output N Multiplexed Outputs	Rising Edge of SCLK	Latched DIN or 1	Yes	Yes	No
G	N Parallel Latched Inputs N Multiplexed Outputs	Falling Edge of Load	Latched DIN or 1	Yes	No	No

Table 3

NV Register Area for Typical Memory & Data I/O Configurations

NV Latch Type = Single Ended

I/O Configuration			Redundant EE Cell?	NV Register Area (K sq. um) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	22.5	41.5	79.4	155.3
B	N Parallel Bi-Directional I/O's		Yes	22.5	41.5	79.4	155.3

Table 4A

NV Latch Type = Differential

I/O Configuration			Redundant EE Cell?	NV Register Area (K sq. um) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	24.0	44.2	84.7	165.6
B	N Parallel Bi-Directional I/O's		No	24.0	44.2	84.7	165.6
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	No	26.6	49.0	93.8	183.5
D	1 Serial Input	N Parallel Tri-State Outputs	No	27.6	50.9	97.5	190.7
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	No	28.5	52.5	100.6	196.7
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	No	38.1	70.2	134.4	262.8
G	N Parallel Latched Inputs	N Multiplexed Outputs	No	(31*)	(58*)	(111*)	(218*)
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	29.8	54.9	105.1	205.5
B	N Parallel Bi-Directional I/O's		Yes	29.8	54.9	105.1	205.5
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	Yes	32.4	59.6	114.2	223.3
D	1 Serial Input	N Parallel Tri-State Outputs	Yes	33.4	61.6	117.9	230.6
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	Yes	34.3	63.2	121.0	236.6
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	Yes	43.9	80.8	154.8	302.7
G	N Parallel Latched Inputs	N Multiplexed Outputs	Yes	(37*)	(69*)	(132*)	(258*)

Table 4B

(*) = Estimated

NV Register Area for Typical Memory & Data I/O Configurations

NV Latch Type = Single Ended

I/O Configuration			Redundant EE Cell?	NV Register Area (sq. mils) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	34.9	64.3	123.2	240.8
B	N Parallel Bi-Directional I/O's		Yes	34.9	64.3	123.2	240.8

Table 5A

NV Latch Type = Cross-Coupled

I/O Configuration			Redundant EE Cell?	NV Register Area (sq. mils) vs. Number of Bits			
Type	Data Inputs	NV Data Outputs		8 Bits	16 Bits	32 Bits	64 Bits
A	N Parallel Inputs	N Parallel Tri-State Outputs	No	37.2	68.6	131.3	256.7
B	N Parallel Bi-Directional I/O's		No	37.2	68.6	131.3	256.7
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	No	41.2	75.9	145.4	284.4
D	1 Serial Input	N Parallel Tri-State Outputs	No	42.8	78.9	151.2	295.6
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	No	44.2	81.5	156.0	305.0
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	No	59.0	108.8	208.4	407.5
G	N Parallel Latched Inputs	N Multiplexed Outputs	No	(49*)	(90*)	(173*)	(339*)
A	N Parallel Inputs	N Parallel Tri-State Outputs	Yes	46.1	85.1	162.9	318.6
B	N Parallel Bi-Directional I/O's		Yes	46.1	85.1	162.9	318.6
C	N Parallel Latched Inputs	N Parallel Tri-State Outputs	Yes	50.2	92.5	177.1	346.3
D	1 Serial Input	N Parallel Tri-State Outputs	Yes	51.8	95.4	182.8	357.4
E	1 Serial Input	1 Serial Output + N Parallel Tri-State Outputs	Yes	53.1	98.0	187.6	366.9
F	1Serial Input	1 Serial Output + N Multiplexed Outputs	Yes	68.0	125.3	240.0	469.3
G	N Parallel Latched Inputs	N Multiplexed Outputs	Yes	(58*)	(107*)	(205*)	(400*)

Table 5B

(*) = Estimated