CSS ALib — Pch Input, Class AB Output Amplifier (Amp_AB_P1E)

CSS Analog Library

General Description

This analog macro cell is a single supply, general purpose operational amplifier. It contains a folded cascode, P_{CH} differential input stage and a class AB output stage. The common mode input range extends from GND to (V_{POS} – 0.8V). The output stage is capable of driving off-chip loads of 1KΩ and 50pF. The amplifier is internally compensated and is unity gain stable. An "Enable" input is included to allow the amplifier to be placed into a low (~ zero) power mode.

Features / Specifications

Process: AMI C5 (requires Double Poly & Double Metal)
Temperature range: 0°C to +70°C
Supply Voltage: 2.7V to 5.5V
Supply Current:
- Shutdown current < 10nA
- Active current - 20µA (IBias = 1uA)
- Active current - 94µA (IBias = 5uA)
- Active current - 315µA (IBias = 25uA)

Common Mode Input Range – GND to (V_{POS}-0.8V)
Gain Bandwidth Product:
- ~ 0.3 MHz at IBias = 1uA
- ~ 1 MHz at IBias = 5uA
- ~ 2.5 MHz at IBias = 25uA

Slew Rate:
- ~ 0.25 V/us at IBias = 1uA
- ~ 1.0 V/us at IBias = 5uA
- ~ 5.0 V/us at IBias = 25uA

Physical Layout Size:
- 260 x 70 microns (10 x 3 mils)

Pin Description

Power Pins

VPOS	Positive supply voltage.
VSS	Ground.

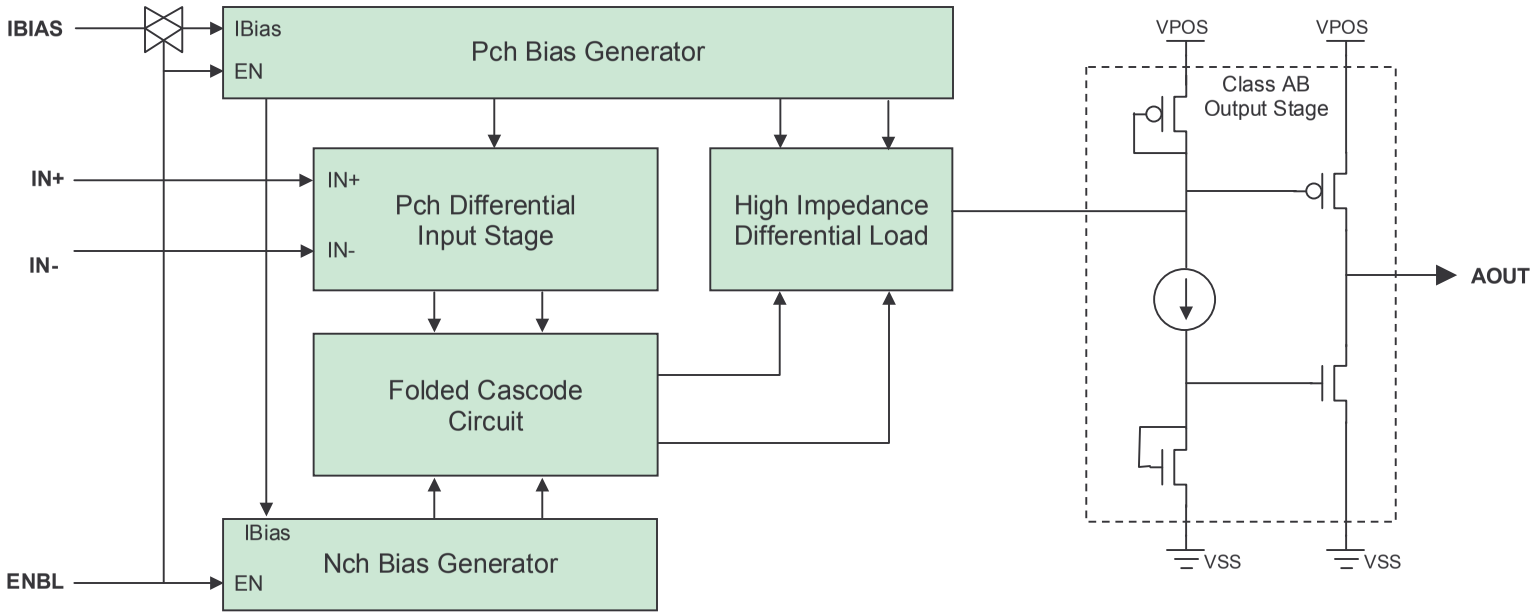
Control Pins

ENBL	"Enable" input - Enables the amplifier when high.

Signal Pins

IB_P	Input Bias Current to Pch Mirror
IN_P	Non-Inverting input
IN_N	Inverting input
AOUT	Amplifier output

Simplified Schematic



DC Electrical Specifications (from SPICE)

Operating Conditions:

Temperature Range = +0ºC to +70ºC (Typical = +25ºC)

Parameter	Symbol	Test Conditions	IBias	VPOS = 3.0V			VPOS = 5.0V			Units
				Min.	Typical	Max.	Min.	Typical	Max.	
Supply current (Shutdown)	I_{DDSD}	ENBL = 0, No load	X		< 0.01			< 0.01		µA
Supply current (Active)	I_{DD}	ENBL = 1, No load	1 µA		20			22		µA
		Unity Gain, V_{IN} = VPOS/2	5 µA		94			101		µA
			25 µA		316			475		µA
Input bias current (V_{IN+}, V_{IN-})	I_{IB}	0V < V_{IN} < VPOS	X		< 1			< 1		pA
Common Mode	V_{CMIR}	Unity Gain, R_L = 1MΩ	1 µA	0		2.12	0		4.08	V
Input Range		$\|V_{IN} - V_{OUT}\|$ < 1mV	5 µA	0		2.10	0		4.05	V
			25 µA	0		2.10	0		4.02	V
Input Offset Voltage	V_{IOS}	Unity Gain, V_{IN} = VPOS/2	1 µA		80			195		uV
		R_L = 1MΩ	5 µA		40			100		uV
		No device mismatch	25 µA		30			70		uV
High Level	V_{OH}	Gain = 2.0, V_{IN} = VPOS/2	1 µA		2.82			4.89		V
Output Voltage		I_{OH} = -0.5mA	5 µA		2.82			4.89		V
			25 µA		2.80			4.89		V
Low Level	V_{OL}	Unity Gain, V_{IN} = 0V	1 µA		0.20			0.12		V
Output Voltage		I_{OH} = 0.5mA	5 µA		0.20			0.12		V
			25 µA		0.20			0.12		V
Differential Voltage	A_{V0}	V_{IN} = VPOS/2	1 µA		148			134		dB
Gain (DC)		R_L = 1MΩ	5 µA		140			140		dB
			25 µA		131			133		dB
Common Mode	V_{CMRR0}	Unity Gain, V_{IN} = VPOS/2	1 µA		-104			-102		dB
Rejection Ratio (DC)		R_L = 1MΩ	5 µA		-110			-113		dB
			25 µA		-90			-132		dB
Power Supply	V_{PSRR0}	Unity Gain, V_{IN} = VPOS/2	1 µA		-85			-85		dB
Rejection Ratio (DC)		R_L = 1MΩ	5 µA		-90			-90		dB
			25 µA		-98			-92		dB

Table 1A

AC Electrical Specifications (from SPICE)

Operating Conditions:

Temperature Range = +0ºC to +70ºC (Typical = +25ºC)

Parameter	Symbol	Test Conditions	IBias	VPOS = 3.0V			VPOS = 5.0V			Units
				Min.	Typical	Max.	Min.	Typical	Max.	
Turn-On Time ENBL = 0 to 1	t_{ON}	Unity Gain, V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 50pF $\|V_{IN} - V_{OUT}\| < 0.1\%$	1 µA		10.8			14.5		µs
			5 µA		3.1			3.7		µs
			25 µA		1.2			1.1		µs
Turn-Off Time ENBL = 1 to 0	t_{OFF}	Unity Gain, V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 50pF IDD < 1 µA	1 µA		< 0.1			< 0.1		µs
			5 µA		< 0.1			< 0.1		µs
			25 µA		< 0.1			< 0.1		µs
Gain Bandwidth Product	AV_{BWP}	V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 50pF	1 µA		0.33			0.33		MHz
			5 µA		1.1			1.1		MHz
			25 µA		2.5			2.7		MHz
Phase Margin	Φ_M	V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 50pF	1 µA		58			60		degrees
			5 µA		51			52		degrees
			25 µA		43			52		degrees
Gain Bandwidth Product	AV_{BWP}	V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 10pF	1 µA		0.36			0.36		MHz
			5 µA		1.25			1.25		MHz
			25 µA		3.25			3.25		MHz
Phase Margin	Φ_M	V_{IN} = VPOS/2 R_L = 1MΩ, C_L = 10pF	1 µA		76			77		degrees
			5 µA		74			74		degrees
			25 µA		72			78		degrees
Differential Voltage Gain	A_{V1}	V_{IN} = VPOS/2 at 10 kHz R_L = 1MΩ, C_L = 50pF	1 µA		31			31		dB
			5 µA		42			42		dB
			25 µA		50			50		dB
Common Mode Rejection Ratio	V_{CMRR}	Unity Gain V_{IN} = VPOS/2 at 10 kHz R_L = 1MΩ, C_L = 0pF	1 µA		-31			-31		dB
			5 µA		-42			-42		dB
			25 µA		-50			-50		dB
Power Supply Rejection Ratio	V_{PSRR}	Unity Gain, V_{IN} = VPOS/2 at 10 kHz R_L = 1MΩ, C_L = 0pF	1 µA		-37			-38		dB
			5 µA		-48			-49		dB
			25 µA		-57			-57		dB

Table 1B

AC Electrical Specifications (from SPICE)

Operating Conditions:

Temperature Range = +0ºC to +70ºC (Typical = +25ºC)

Parameter	Symbol	Test Conditions	IBias	VPOS = 3.0V			VPOS = 5.0V			Units
				Min.	Typical	Max.	Min.	Typical	Max.	
Positive Slew Rate	SR_P	Unity Gain, R_L = 1MΩ	1 µA		0.23			0.23		V/µs
C_L = 50pF		V_{IN} = 0.5V to 1.5V, VDD = 3V	5 µA		1.1			1.15		V/µs
		V_{IN} = 1.5V to 2.5V, VDD = 5V	25 µA		5.3			5.4		V/µs
Negative Slew Rate	SR_N	Unity Gain, R_L = 1MΩ	1 µA		0.23			0.23		V/µs
C_L = 50pF		V_{IN} = 1.5V to 0.5V, VDD = 3V	5 µA		1.2			1.2		V/µs
		V_{IN} = 2.5V to 1.5V, VDD = 5V	25 µA		5.2			5.8		V/µs
Positive Slew Rate	SR_P	Unity Gain, R_L = 1MΩ	1 µA		0.22			0.23		V/µs
C_L = 10pF		V_{IN} = 0.5V to 1.5V, VDD = 3V	5 µA		1.1			1.15		V/µs
		V_{IN} = 1.5V to 2.5V, VDD = 5V	25 µA		5.6			5.7		V/µs
Negative Slew Rate	SR_N	Unity Gain, V_{IN} = 1.5V to 0.5V	1 µA		0.23			0.24		V/µs
C_L = 10pF		V_{IN} = 1.5V to 0.5V, VDD = 3V	5 µA		1.2			1.2		V/µs
		V_{IN} = 2.5V to 1.5V, VDD = 5V	25 µA		5.7			5.8		V/µs
Total Response Time	t_S	Unity Gain, V_{STEP} = ±1V	1 µA		7.6			5.6		µs
C_L = 50pF		R_L = 1MΩ	5 µA		2.5			2.0		µs
		$\|V_{IN} - V_{OUT}\|$ < 0.1%	25 µA		1.0			0.7		µs
Total Response Time	t_S	Unity Gain, V_{STEP} = ±1V	1 µA		5.4			5.4		µs
C_L = 10pF		R_L = 1MΩ	5 µA		1.3			1.3		µs
		$\|V_{IN} - V_{OUT}\|$ < 0.1%	25 µA		0.37			0.33		µs

Table 1C

Typical Characteristics (from SPICE)

Table of Charts (VPOS = 2.5V to 5.5V)

Parameter	Symbol	Test Conditions	Secondary Parameters	PDF File
Supply Current (normalized)	I_{DD}	Unity Gain, No Load, V_{IN} = VPOS/2	vs. VPOS & IBias	Amp_ABP1_IDDvsVPOS
High Level Output Current	I_{OH}	Gain = 2.0, V_{IN} = VPOS/2, Vout = VPOS - 0.1V	vs. VPOS	Amp_ABP1_ISOURCEvsVPOS
Low Level Output Current	I_{OL}	Unity Gain, V_{IN} = 0V, Vout = 0.1V	vs. VPOS	Amp_ABP1_ISINKvsVPOS

Table 2A

Table of Charts (VPOS = 3V)

Parameter	Symbol	Test Conditions	Secondary Parameters	PDF File
Supply Current	I_{DD}	Unity Gain, No Load	vs. V_{IN} & IBias	Amp_ABP1_IDDvsVIN_3V
Input Voltage Range	V_{CMIR}	Unity Gain, IBias = 1uA, R_L = 1K, 10K, 100K & 1MΩ	vs. V_{IN} & IBias	Amp_ABP1_VOUTvsVIN_RL_3V
Input Offset Voltage (ideal)	V_{IOS}	Unity Gain, R_L = 1MΩ, No FET mismatch	vs. V_{IN} & IBias	Amp_ABP1_VIOSvsVIN_3V
High Level Output Voltage	V_{OH}	Gain = 2.0, V_{IN} = VPOS/2	vs. I_{OUT} & IBias	Amp_ABP1_VOHvsIOUT_3V
Low Level Output Voltage	V_{OL}	Unity Gain, V_{IN} = 0V	vs. I_{OUT} & IBias	Amp_ABP1_VOLvsIOUT_3V
Output Impedance	Z_{OUT}	Unity Gain, V_{IN} = VPOS/2	vs. Frequency & IBias	Amp_ABP1_ZOUTvsFREQ_3V
Power Supply Rejection Ratio	PSRR	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ	vs. Frequency & IBias	Amp_ABP1_PSRRvsFREQ_3V
Common Mode Rejection Ratio	CMRR	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ	vs. Frequency & IBias	Amp_ABP1_CMRRvsFREQ_3V
Differential Voltage Gain & Phase	A_V & Φ_M	V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 50pF	vs. Frequency & IBias	Amp_ABP1_GAINvsFREQ_3V_50pF
Differential Voltage Gain & Phase	A_V & Φ_M	V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 10pF	vs. Frequency & IBias	Amp_ABP1_GAINvsFREQ_3V_10pF
Large Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_LgSTEPvsIBIAS_3V_50pF
Large Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_LgSTEPvsIBIAS_3V_10pF
Small Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_SmSTEPvsIBIAS_3V_50pF
Small Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_SmSTEPvsIBIAS_3V_10pF
Turn On Response	t_{ON}	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_TURNONvsIBIAS_3V_50pF
Turn On Response	t_{ON}	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_TURNONvsIBIAS_3V_10pF

Table 2B

Typical Characteristics (from SPICE)

Table of Charts (VPOS = 5V)

Parameter	Symbol	Test Conditions	Secondary Parameters	PDF File
Supply Current	I_{DD}	Unity Gain, No Load	vs. V_{IN} & IBias	Amp_ABP1_IDDvsVIN_5V
Input Voltage Range	V_{CMIR}	Unity Gain, IBias = 1uA, R_L = 1K, 10K, 100K & 1MΩ	vs. V_{IN} & IBias	Amp_ABP1_VOUTvsVIN_RL_5V
Input Offset Voltage (ideal)	V_{IOS}	Unity Gain, R_L = 1MΩ, No FET mismatch	vs. V_{IN} & IBias	Amp_ABP1_VIOSvsVIN_5V
High Level Output Voltage	V_{OH}	Gain = 2.0, V_{IN} = VPOS/2	vs. I_{OUT} & IBias	Amp_ABP1_VOHvsIOUT_5V
Low Level Output Voltage	V_{OL}	Unity Gain, V_{IN} = 0V	vs. I_{OUT} & IBias	Amp_ABP1_VOLvsIOUT_5V
Output Impedance	Z_{OUT}	Unity Gain, V_{IN} = VPOS/2	vs. Frequency & IBias	Amp_ABP1_ZOUTvsFREQ_5V
Power Supply Rejection Ratio	PSRR	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ	vs. Frequency & IBias	Amp_ABP1_PSRRvsFREQ_5V
Common Mode Rejection Ratio	CMRR	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ	vs. Frequency & IBias	Amp_ABP1_CMRRvsFREQ_5V
Differential Voltage Gain & Phase	A_V & Φ_M	V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 50pF	vs. Frequency & IBias	Amp_ABP1_GAINvsFREQ_5V_50pF
Differential Voltage Gain & Phase	A_V & Φ_M	V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 10pF	vs. Frequency & IBias	Amp_ABP1_GAINvsFREQ_5V_10pF
Large Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_LgSTEPvsIBIAS_5V_50pF
Large Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_LgSTEPvsIBIAS_5V_10pF
Small Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_SmSTEPvsIBIAS_5V_50pF
Small Signal Step Response	SR & t_S	Unity Gain, V_{STEP} = ±1V, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_SmSTEPvsIBIAS_5V_10pF
Turn On Response	t_{ON}	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 50pF	vs. IBias	Amp_ABP1_TURNONvsIBIAS_5V_50pF
Turn On Response	t_{ON}	Unity Gain, V_{IN} = VPOS/2, R_L = 1MΩ, C_L = 10pF	vs. IBias	Amp_ABP1_TURNONvsIBIAS_5V_10pF

Table 2C