CSS NVM 2K x 8 EEPROM Macro

CSS NV Memory Library

General Description

This nonvolatile memory is a 16K bit EEPROM macro cell, organized 2K by 8. The memory core is a two dimensional XY array of EE cells. Each cell holds one bit of data and contains two transistors: a floating gate memory FET and a standard, low voltage FET used to access the memory FET during Read. Programming is accomplished via Fowler-Nordheim tunneling. (The high voltage required for programming is supplied by a charge pump, which is a separate circuit block.)

The Read mode is synchronous. The data output signals have tri-state output drivers to facilitate either a single or dual port architecture. Two special test modes have been included to provide a means to insure the integrity of the nonvolatile data. The "Margin" test mode allows the current used to sense the state of the EE cell to be increased or decreased. This test can be used to insure that there is an adequate threshold shift in the EE cell to read correctly. The second test mode provides direct access to the EE cell current.

Program modes include: Page Erase, Block Erase and Page Write. To decrease the time required to program new data, writing is performed one page at a time. (One page equals eight bytes, which corresponds to one physical row of memory.) A data (DIN) register is included in the EEPROM and holds eight bytes of data. It is written like a RAM. During a Page Write operation, the contents of this register is programmed into the selected row of memory.

Features

- Low Power and Wide Supply Range
- Memory Architecture:
  - Memory size = 16K (2K x 8) bits
  - Organized into 256 pages, each page contains 8 words
- Operating Modes:
  - Store Modes: Loan DIN Register, Block Erase, Page Erase, Page Write
  - Read Modes: Synchronous Read
  - Test Modes: Margin Read and EE Cell Current Test
- Output Driver:
  - Tri-State for Single or Dual Port

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Specification Summary

Process: AMI C5F (requires double Poly, double layer metal and thick gate oxide)
Temperature range = 0ºC to 50ºC
Supply Voltage:
- 2.0V (typical), Range = ±10%

Supply Current:
- Standby current = <100nA
- Read current = <50µA
- Store current = <100µA (peak), <50µA (average)

Memory Size:
- Physical size ~ 2000µm x 1050µm

Read Access Time:
- Access time < 10µs

Store Mode:
- Store time < 100 ms
- Endurance (number of Store cycles) >10K
- Data Retention > 50 years at 40ºC
- VPP supplied by a charge pump (separate circuit block)

Address & Data I/O
- Row (Page) address = RADD[7:0]
- Column (Byte) address = CADD[2:0]
- Data In/Data Out are dual port
- Data outputs, tri-state (separate output enable (OE) signal)

External reference current required
- I_{REF} = 0.3µA ±25%

Pin Descriptions

Power Pins

VDD	Positive supply voltage.
VSS	Ground.
VPP	Programming voltage (from the VPP Generator, a separate block)

Control Pins

CE	Chip Enable. Enables all functions except Load Data. (Pulsed high after all other signals are stable.)
READ	Enables the Read mode. (Active high.)
PRGM	Enables the Erase and Write modes. (Active high.)
E_WB	Selects between the Erase and Write modes. (Logic high = Erase.)
BLOCK	Enables Block Erase mode. (Active high.)
LOADB	Strobes DIN data into D latches, 8 bits at a time. (Active low.)
MRGN_EN	Enables direct access to the Isense current used by the sense amps. (Active high.)
TMEN	Enables direct access to the EE Cell Read current. (Active high.)
OE	Output enable control. Enables Data Out output driver. (Logic low = High Z.)
PROGB	Output from EEPROM Control block. It enables the VPP Generator. (Active low.)

Address Pins

ADDR[10:0]	Row and column address lines. Used to select 1 of 2048 address locations.
RADD[7:0]	Row address lines. (ADDR[10:3]) Used to select 1 of 256 rows or pages. (LSB = RADD0)
CADD[2:0]	Column address lines. (ADDR[2:0]) Used to select 1 of 8 bytes within each page. (LSB = CADD0)

Data I/O Pins

DIN[7:0]	Data input lines, 8 total. Used to enter data into the D latches.
DOUT[7:0]	Data output lines, 8 total. (These are tri-state outputs.)
I_MRGN	Test current when Margin Mode is active.

Operating Modes

Standby	Standby/Low current mode
Read	Accesses one word (8 bits) of nonvolatile data from the EE memory array.
Margin	Allows indirect check of the EE Cell Vt.
Test Mode	Allows direct access to each EE Cell Read current. (Requires analog path from $DOUT_N$ to an external test pin.)
Load Data	Input data is strobed into data latches. 8 bits are loaded at a time. Column address, CADD[2:0], selects which word within the page is loaded.
Page Erase	Erases one page (8 words). The page to be erased is selected with row address lines RADD[7:0]. An erased bit equals a logic zero.
Block Erase	Erases all 256 pages.
Write	Programs one page (8 words) with the data stored in the data latches. This operation can only change a logic zero to a one.

A summary of the operating modes is provided in Tables 1 & 2.

Read Modes

PRGM = 0, BLOCK = 0, LOADB = 1, EWB = X (Don't Care), DIN = X

Mode	Description	CE	READ	OE	MRGN_EN	TMEN	I_MRGN	$ADDR_N$	$DOUT_N$
Standby	Low Current Standby	0	0	0	0	0	X	X	High Z
Read	Normal Read Mode	1	1	1	0	0	X	Valid	$DOUT_N$
MarginE Read	Read with Margin (Erased state)	1	1	1	1	0	$+I_M$ (source)	Valid	0 = Pass
MarginW Read	Read with Margin (Written state)	1	1	1	1	0	$-I_M$ (sink)	Valid	1 = Pass
Test Mode	Measure EE Cell Current	1	1	0	1	1	VDD	Valid	I_{EE} Cell

Table 1

Store Modes

READ = 0, OE = 0, MRGN_EN = 0, TMEN = 0, I_MRGN = Don't Care, DOUT = High Z (see Note 1)

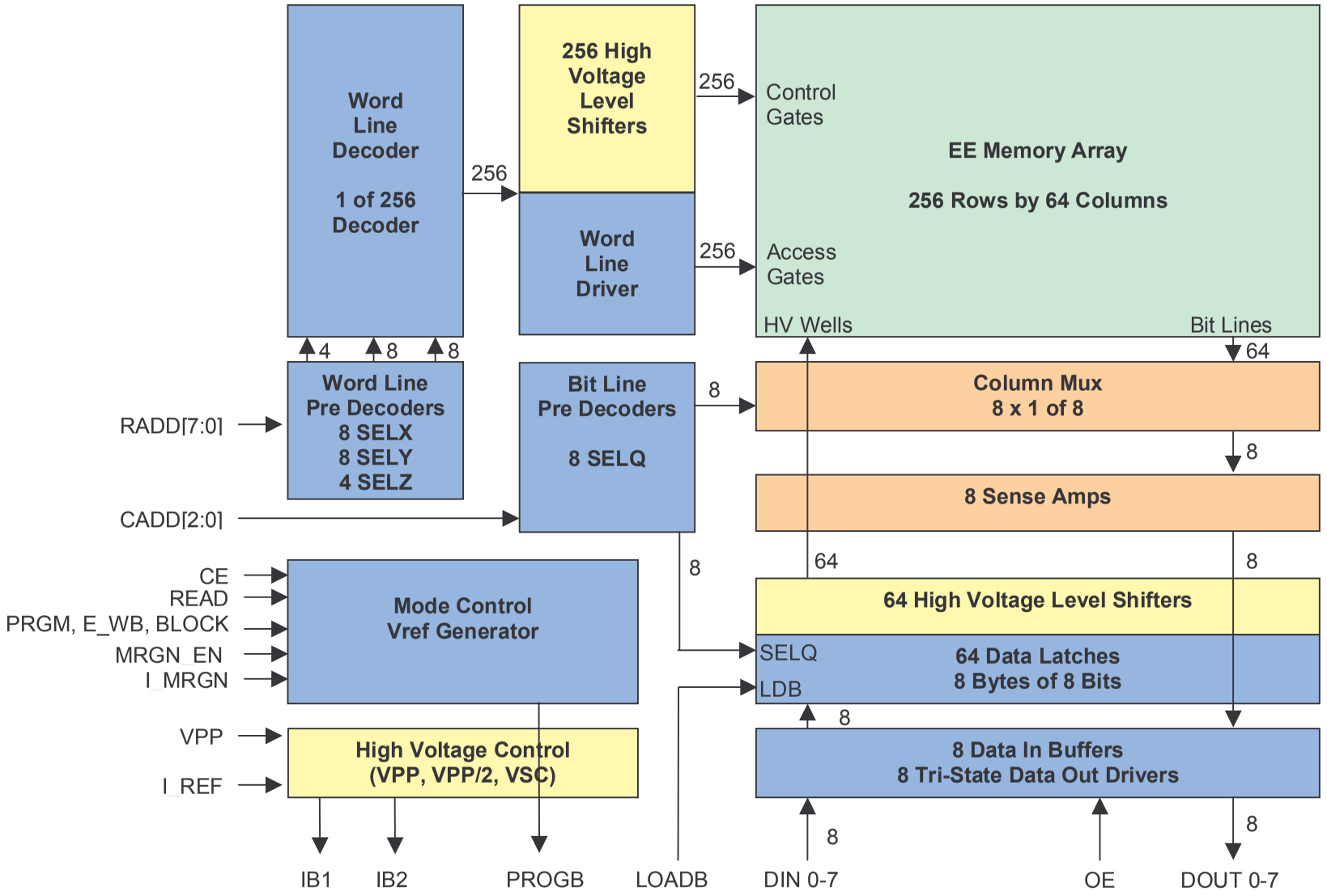
Mode	Description	CE	PRGM	EWB	BLOCK	LOADB	$CADD_N$	$RADD_N$	DIN_N
Load Data	Load DIN Latches (1 byte)	0	0	X	X	0	Valid	X	Valid
Page Erase	Erase 1 page (one row)	1	1	1	0	1	X	Valid	X
Block Erase	Erase all pages	1	1	1	1	1	X	X	X
Page Write	Write 1 page	1	1	0	0	1	X	Valid	X

Table 1

Notes:

1) If OE = 1 during any mode other than Read or Margin, DOUT = 0.
2) CADD ≡ Column Address (ADDR[2:0])
3) RADD ≡ Row Address (ADDR[10:3])
4) A more detailed description of the Margin and Test modes is provided in Application Note #1.

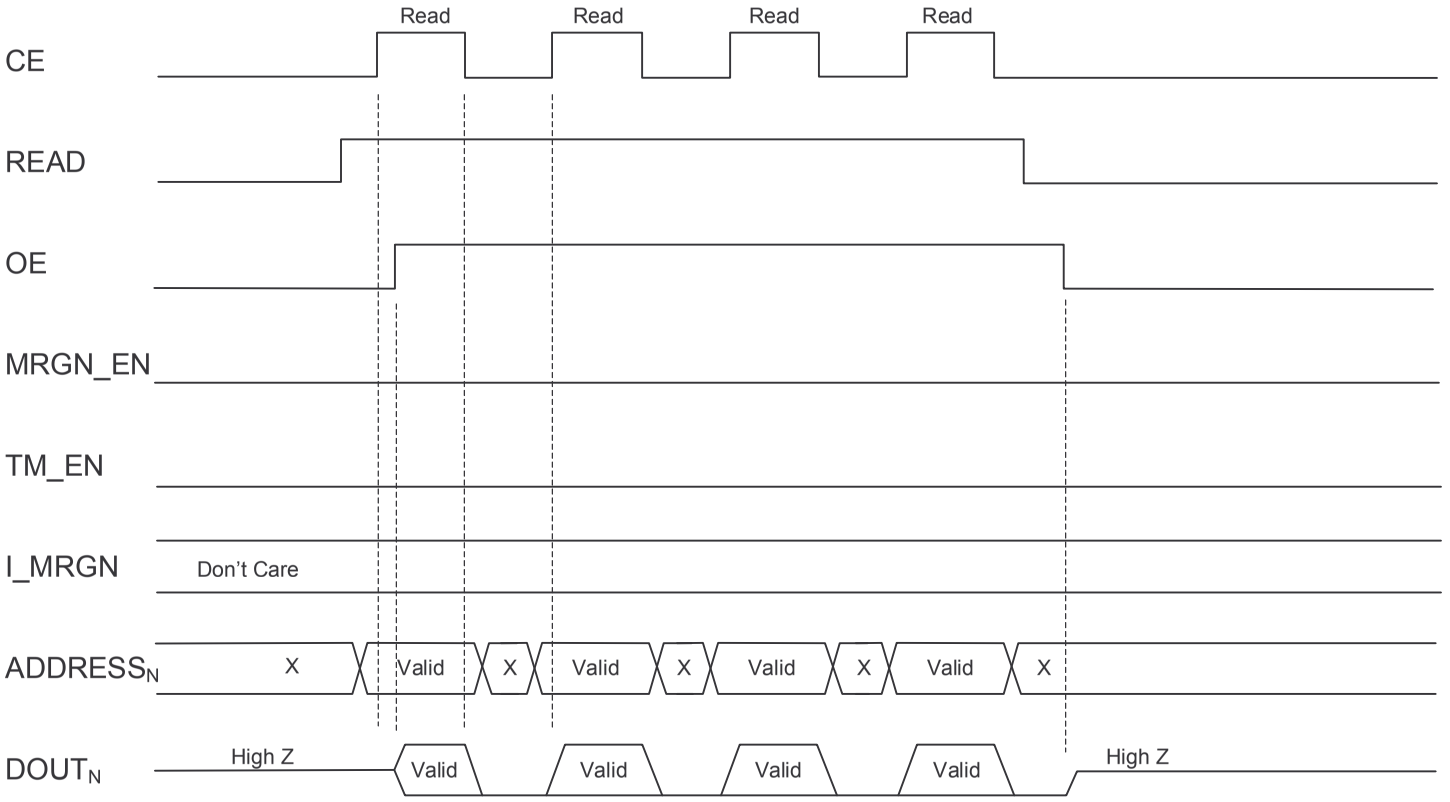
EEPROM Block Diagram



Timing Diagrams

Read 4 Bytes

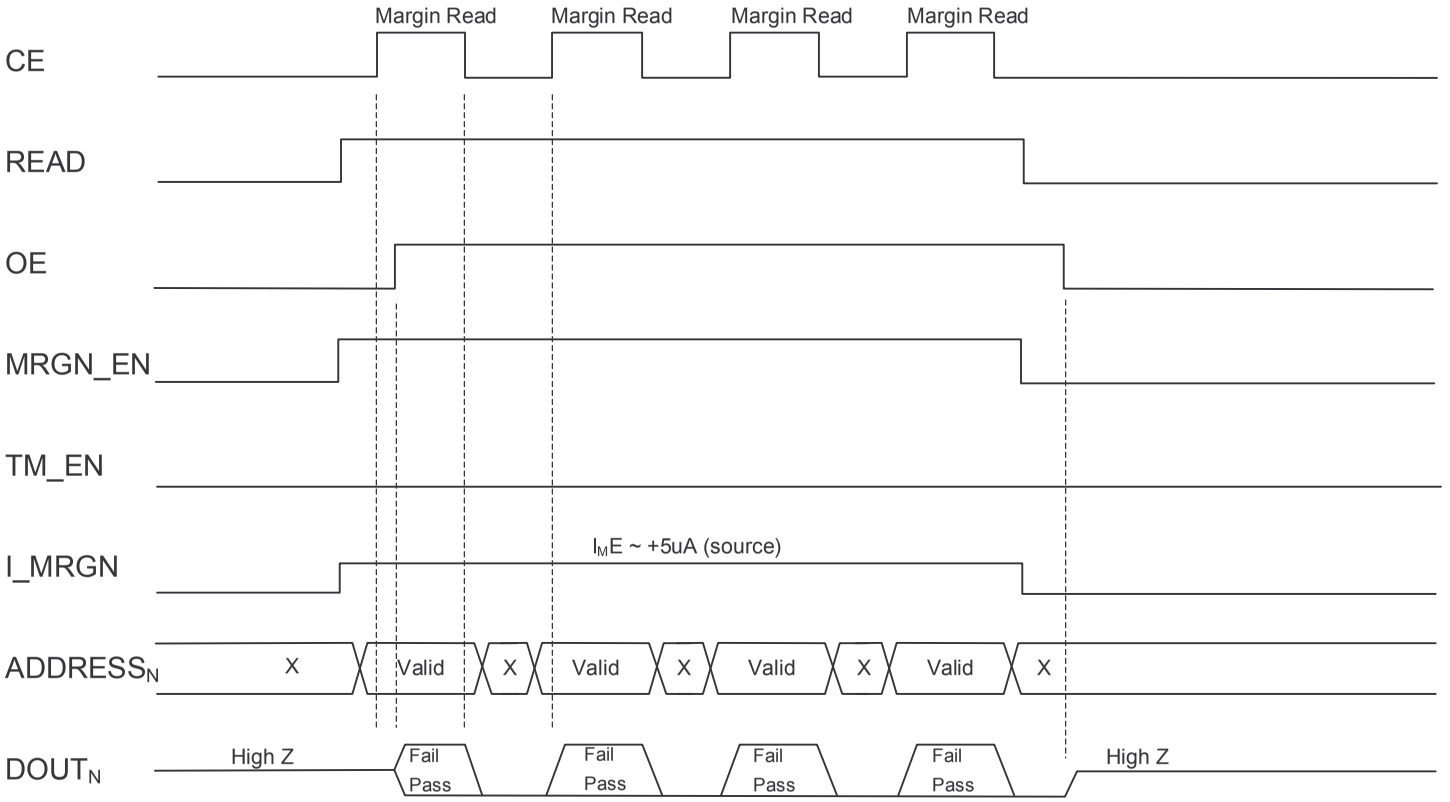
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



Timing Diagrams

Read with Margin (4 Erased Bytes)

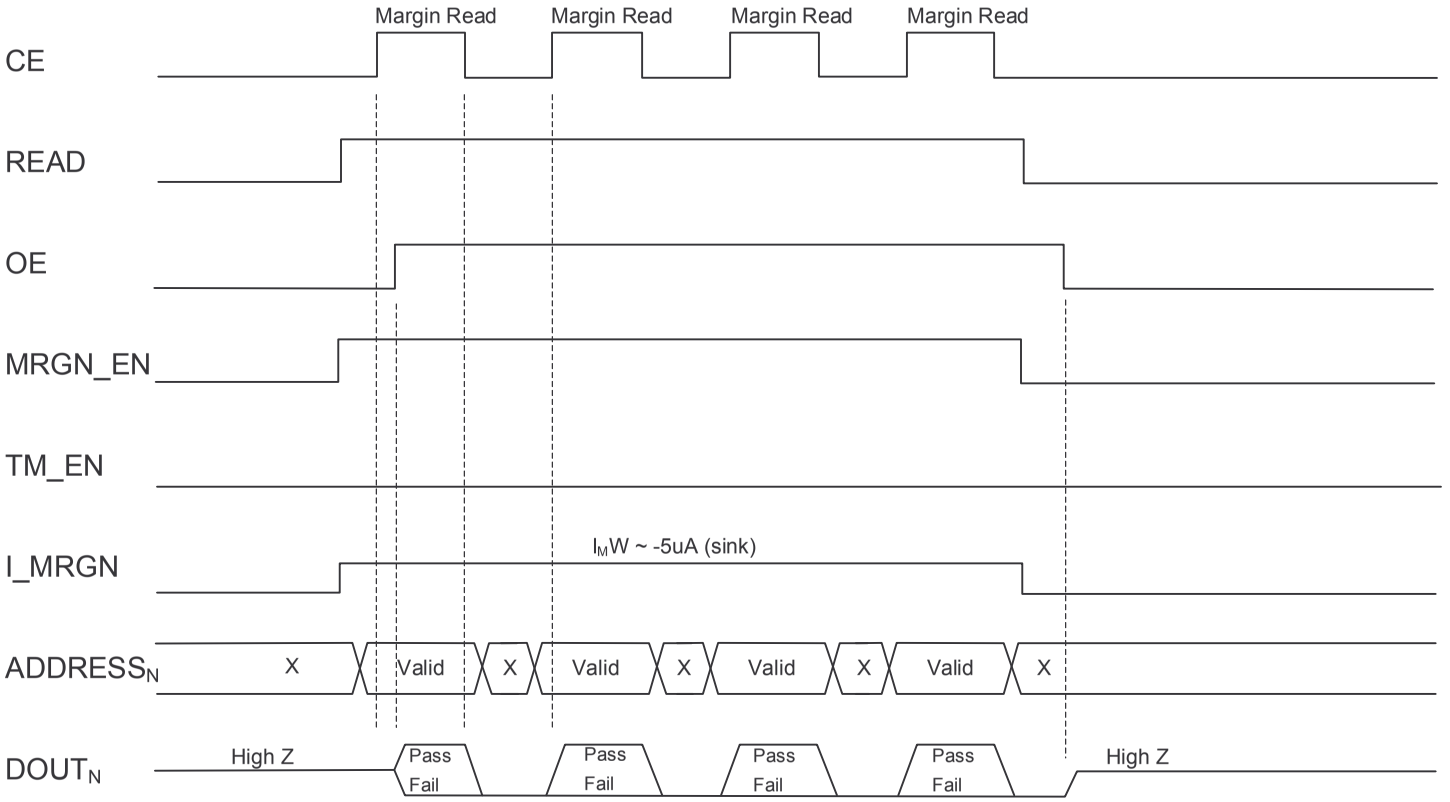
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



Timing Diagrams

Read with Margin (4 Written Bytes)

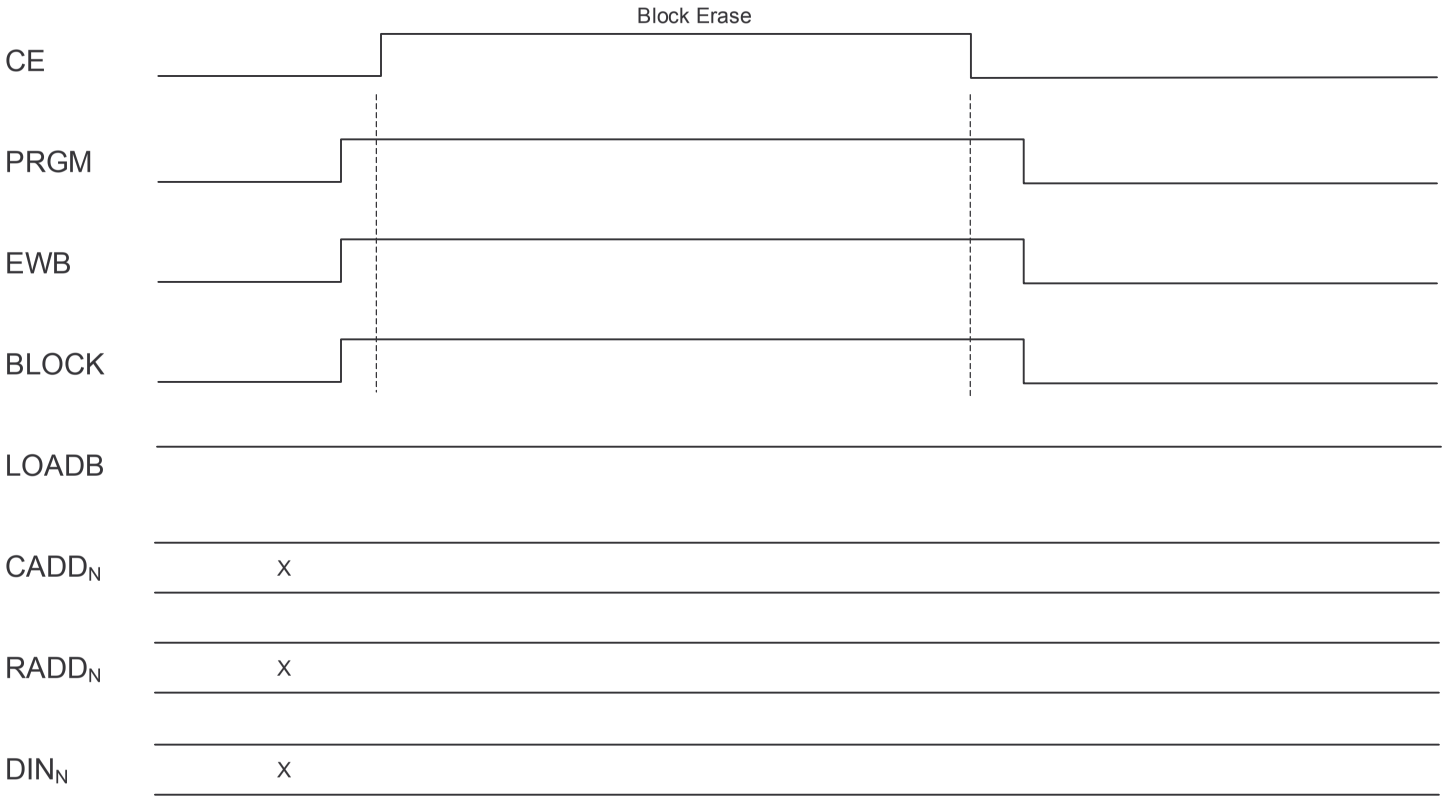
PRGM = 0, BLOCK = 0, LOADB = 1, EWB = Don't Care, DIN = Don't Care



Timing Diagrams

Block Erase

READ = 0, LOADB = 1, MRGN_EN = 0, TM_EN = 0, OE = 0, I_MRGN = Don't Care, DIN = Don't Care, DOUT = High Z



Timing Diagrams

Typical Page Program Sequence (Page Erase, Load Data, Page Write)

READ = 0, LOADB = 1, MRGN_EN = 0, TM_EN = 0, OE = 0, I_MRGN = Don't Care, DIN = Don't Care, DOUT = High Z